Statistical Comparison and Evaluation of Pilot Protection Schemes

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STATISTICAL COMPARISON AND EVALUATION OF PILOT PROTECTION SCHEMES

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INTRODUCTION

Pilot protection schemes speed fault clearing. A variety of schemes has been developed to meet the requirements of dependability, security, cost, and other factors. For example, blocking schemes trip fast for in-section faults, at the risk of misoperating for external faults if the channel fails. Permissive schemes trade off the risk of overtripping for the risk of a time-delayed trip for an internal fault.

We quantify the likelihood of misoperations (overtripping, time-delayed tripping), fault resistance coverage, operating times, and complexity for several popular protection schemes. We propose a new scheme, which provides faster operation, better fault resistance coverage, and minimizes the risks of misoperations.

MEASURES OF SCHEME PERFORMANCE

We selected security, dependability, operating time, fault resistance coverage, and complexity as five key factors in comparing pilot protection schemes.

Security

Security measures the ability of a scheme to operate only for intended faults. We developed Markov models to estimate the lack of security as a likelihood to operate for out-of-section faults.

Dependability

Dependability is confidence that the scheme responds to all internal faults. The same Markov models help us estimate the lack of dependability as a likelihood of a pilot scheme failure to operate for in-section faults.

Operating Time

A fault is not cleared until the protection at both line ends has successfully operated. Our measure of operating time is from fault inception until both ends clear.

Fault Resistance Coverage

Fault resistance coverage is a measure of sensitivity. We assume that directional overcurrent elements are used, which have a 0.5 A pickup setting. We further assume that this setting (not the directional element) governs the element sensitivity.

Figures of Merit

We will develop two figures of merit for the pilot schemes. The first one is the sum of the misoperations expected per year resulting in overtripping (loss of security) and resulting in time delayed tripping (loss of dependability). A simple sum implies equal cost factors for an overtrip and for a time-delayed trip. Other weights could be used. Smaller sums indicate more reliable schemes.

The second figure of merit is the average clearing time divided by the total fault resistance coverage. Faster, more sensitive schemes have lower (better) figures of merit.

Complexity

Scheme complexity is a measure of the zones, timers, and additional logic required to implement the protection. More complex schemes may be more costly or difficult to implement.

SECURITY AND DEPENDABILITY

Early communication-aided schemes used channels of questionable quality. An important consideration in the design of the pilot scheme was the effect of a channel failure on the scheme. Blocking schemes risked overtripping for out-of-section faults occurring while the channel was out. Transfer tripping schemes had higher security, but lower dependability—in-section faults would be cleared with time delay if the channel was out.

Modern communication channels have higher reliability due to improvements in equipment and application guidelines. Yet communication scheme security and dependability remain important performance factors.

To quantify the security and dependability of three popular types of communication schemes, we developed Markov probability models for each. These models produce probabilities that we use to determine the expected time to an overtrip or time-delayed trip. The Markov models are shown in Appendix B.

Figure 1 shows the expected years to an overtrip for Permissive Overreaching Transfer Trip (POTT), Directional Comparison Unblocking (DCUB), and Directional Comparison Blocking (DCB) communication schemes for lines experiencing varying numbers of faults per year.

Figure 2 shows the expected years to a time-delayed trip for each of the schemes.

Table 1 lists the protection scheme performance figures used in the Markov models.

Table 1: Markov Model Variables

Variable	Value Used	Description
MTBF	75 years	Protection Mean Time Between Failures (2 relays, 150 year MTBF each)
ST	0.80	Relay Self-Test Effectiveness
MTBFc	50 years	Channel Equipment MTBF
Fcf	1.0% or 0.1%	Additional Channel Failures Due to Faults
MTRT	2 hours	Mean Time to Test Relay
MTTR	4 hours	Mean Time to Repair Relay or Channel Equipment
MTT79	35 cycles	Longest Reclosing Open Interval, plus Breaker Time
MTTTc	5 cycles	Communication-Aided Fault Clearing Time
Z2D	24 cycles	Zone 2 Fault Clearing Time
Z1D	3.5 cycles	Zone 1 Fault Clearing Time
kz	0.01%	Percent of External Faults That Cause Communication Channel Misoperation

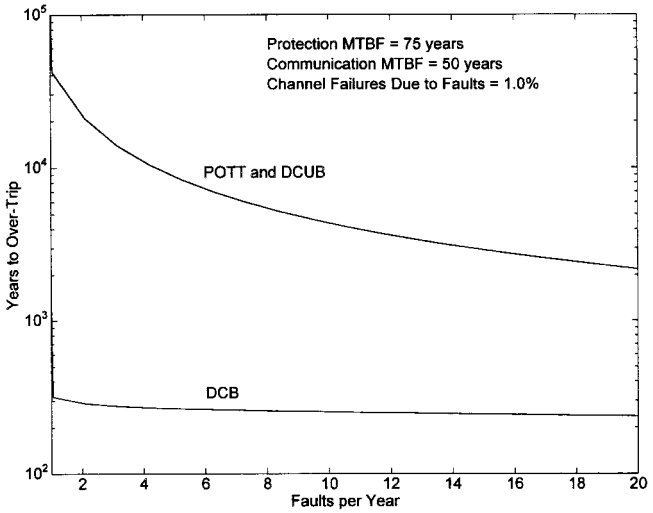

Figure 1: Years to an Overtrip for POTT, DCUB, and DCB Protection Schemes

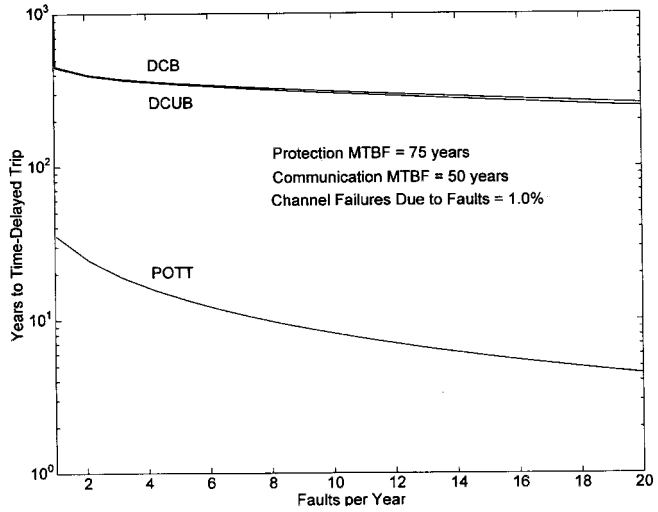

Figure 2: Years to a Time-Delayed Trip for POTT, DCUB, and DCB Protection Schemes

The communication channel routing can have an impact on these figures. For instance, in a transfer-tripping scheme, there is a higher likelihood of a time-delayed trip due to failure to receive permission if the channel is in the line right-of-way. Figure 3 compares two permissive tripping channels. One has a 1.0% chance of being interrupted by an in-section fault and another has a 0.1% chance. These figures suppose that the likelihood of a channel failure for a channel in the faulted line right-of-way is ten times that of a channel on a different path.

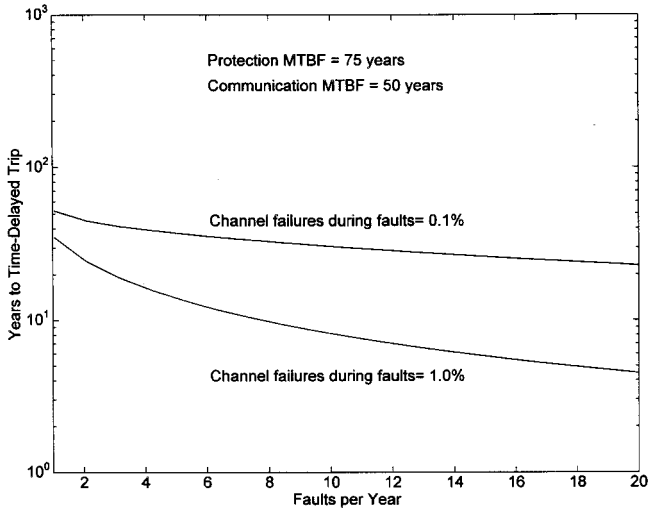

Figure 3: Years to a Time-Delayed Trip for POTT Schemes Having 1.0% and 0.1% Chance of Interruption Due to an In-Section Fault

The best way to use these figures is on a system-wide basis. Assume that a power system consists of 100 lines, all unit protected using identical POTT, DCUB, or DCB protection schemes, and each line experiences ten faults per year. Table 2 shows the expected overtrips per year and time-delayed trips per year, system-wide, for each scheme.

Table 2: Scheme Security and Dependability of a System of 100 Lines Experiencing 1000 Faults per Year

Scheme	Probability of Channel Loss Due to Fault	Overtrips per Year	Time-Delayed Trips per Year	Reliability Figure of Merit (Overtrips and Time-Delayed Trips per Year)
POTT	0.1%	0.022	3.20	3.222
POTT	1.0%	0.022	12.20	12.222
DCB	1.0%	0.380	0.33	0.710
DCUB	1.0%	0.022	0.33	0.352

OPERATING SPEED AND FAULT RESISTANCE COVERAGE

Example Systems

To evaluate protection scheme fault resistance coverage, we considered long line and short line system models, shown in Figures 4 and 6, respectively. In both cases, we considered resistive sensitivity to ground faults only. For Zone 2, we used a sensitive ground directional overcurrent element, set to operate if residual current is above 0.5 A, secondary. For Zone 1, we use a quadrilateral ground distance element, set for 50Ω resistive coverage on a radial system. The 60 percent Zone 1 reach accommodates instrument transformer errors, which may be significant at high values of fault resistance. The Zone 1 and Zone 2 resistive sensitivities are shown for the long line and short line in Figures 5 and 7, respectively. Resistive coverage is shown assuming both line circuit breakers are closed.

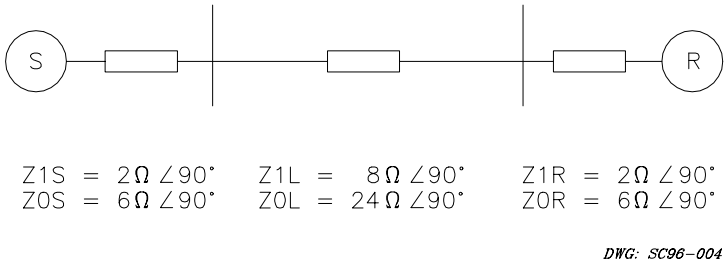

Figure 4: Long Line Example System

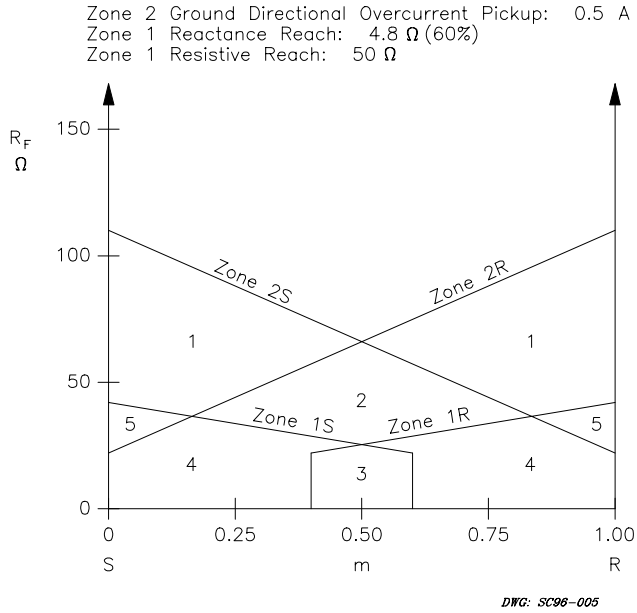

Figure 5: Long Line Resistive Fault Coverage Regions

Table 3: Long Line Coverage Regions

Region 1	37.4 Ω
Region 2	13.7 Ω
Region 3	4.7 Ω
Region 4	25.6 Ω
Region 5	6.6 Ω
Total	**88.0 Ω**

Table 3 lists the area, in ohms, of each region for the long line system. Later, we will see that each protection scheme clears faults in differing times for the various regions. The unit of area measure for these regions is ohms to simplify the comparisons between the long and short lines. To determine the area of each region, we calculated the geometric area in ohms (vertically) times m per unit of the line (horizontally).

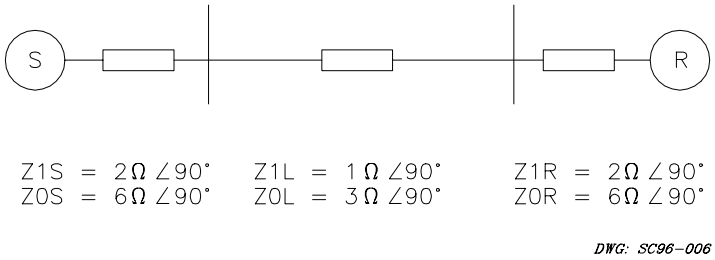

Figure 6: Short Line Example System

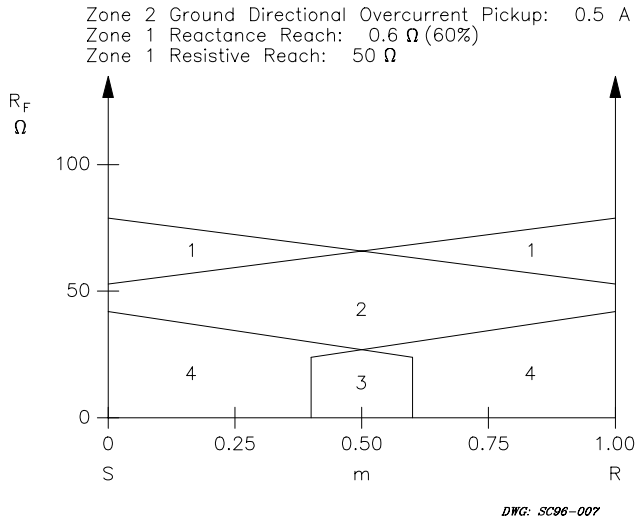

Figure 7: Short Line Resistive Fault Coverage Regions

Table 4: Short Line Coverage Regions

Region 1	13.0 Ω
Region 2	32.0 Ω
Region 3	9.8 Ω
Region 4	17.7 Ω
Total	**72.5 Ω**

In all cases, we assumed the additional parameters shown in Table 5.

Table 5: Additional System Parameters

Element Operating Time	1.0–1.5 cycles
Breaker Clearing Time	2.0 cycles
Channel Operate Delay	1.0 cycle
Zone 2 Time Delay	20 cycles

System Figures of Merit

To compare the schemes we devised a simple figure of merit:

$$\rho_{TR} = \frac{T_{ave}}{Rf} \qquad \text{Equation 1}$$

where:

T_{ave} = the weighted average of fault clearing times for detectable faults.
Rf = the total area of resistive faults detectable by the scheme.

A protection scheme delivering a smaller figure of merit offers better performance.

Time-Stepped Protection

As a baseline for figure of merit comparisons, consider a time-stepped scheme. Figure 8 shows the total fault clearing time for resistive ground faults in various locations on the long line. Faults detected by Zone 1 distance elements at both ends are cleared in a maximum of 3.5 cycles. Faults detected by both Zone 2 time-delayed ground directional overcurrent elements are cleared in 25 cycles. Faults that are detected by only one Zone 2 ground directional overcurrent element are cleared by sequential tripping, in 50 cycles, since the remote Zone 2 cannot detect the fault until the local breaker opens. The figure of merit, ρ_{TR}, for the long line, time-stepped scheme is calculated using Equation 2.

$$\rho_{TR} = \frac{\left(\frac{50\ \text{cyc}\cdot(37.4\ \Omega + 6.6\ \Omega)}{88\ \Omega}\right) + \left(\frac{25\ \text{cyc}\cdot(13.7\ \Omega + 25.6\ \Omega)}{88\ \Omega}\right) + \left(\frac{3.5\ \text{cyc}\cdot 4.7\ \Omega}{88\ \Omega}\right)}{88\ \Omega} = 413 \times 10^{-3} \qquad \text{Equation 2}$$

The average tripping time for all detectable faults is:

T_{ave} = 36.3 cycles

For the short line case, the time-stepped scheme figure of merit and average tripping times are:

$\rho_{TR} = 366 \times 10^{-3}$

T_{ave} = 26.5 cycles

The figures of merit and average tripping times for all schemes are summarized in Tables 6a and 6b.

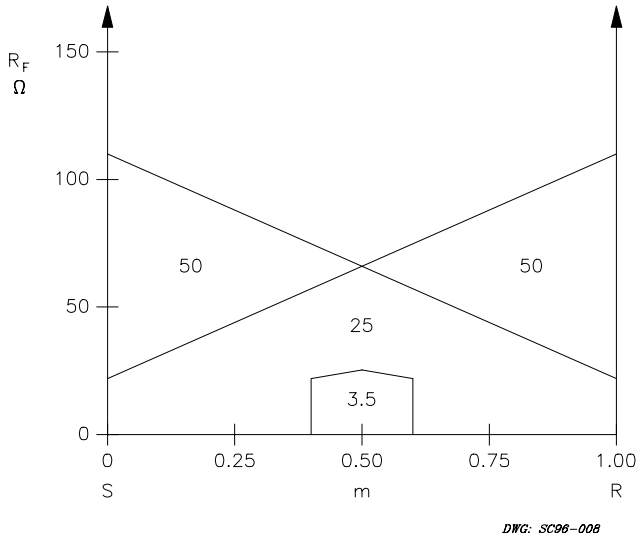

Figure 8: Fault Clearing Times (cycles) for Time-Stepped Protection, Long Line

Direct Underreaching Transfer Trip (DUTT)

Figure 9 shows the fault clearing time areas for DUTT protection. Faults detected by both Zone 1 elements are cleared without time delay at both ends. Faults detected by a single Zone 1 element are cleared with an additional 1-cycle time delay to account for the communication channel delay. In-section Zone 2 faults are cleared simultaneously in 25 cycles, or sequentially in 50 cycles, depending on their location and resistance.

For the long line case, the DUTT figure of merit is calculated:

$$\rho_{TR} = \frac{\left(\frac{50\,\text{cyc}\cdot 37.4\,\Omega}{88\,\Omega}\right)+\left(\frac{25\,\text{cyc}\cdot 13.7\,\Omega}{88\,\Omega}\right)+\left(\frac{4.5\,\text{cyc}\cdot(25.6\,\Omega+6.6\,\Omega)}{88\,\Omega}\right)+\left(\frac{3.5\,\text{cyc}\cdot 4.7\,\Omega}{88\,\Omega}\right)}{88\,\Omega} = 307 \times 10^{-3} \qquad \text{Equation 3}$$

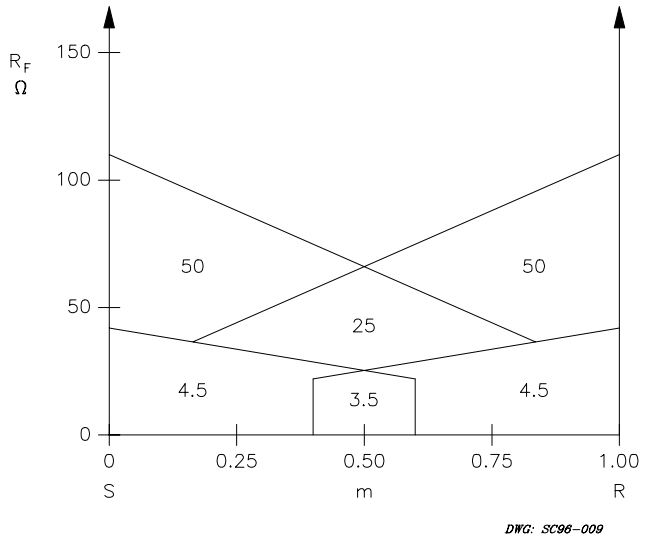

Figure 9: Fault Clearing Times for DUTT Protection, Long Line

Permissive Underreaching Transfer Trip (PUTT)

Figure 10 shows the PUTT fault clearing times. Resistive faults are cleared quickly by the PUTT scheme only if they are detected by both Zone 1 elements, or by the local Zone 1 and remote Zone 2 elements. Faults that fall into the area covered by both Zone 2 elements are cleared in 25 cycles, and faults that fall into a single Zone 2 are cleared sequentially in 25 or 50 cycles.

For the long line case, the PUTT figure of merit is:

$$\rho_{TR} = \frac{\left(\frac{50\,\text{cyc}\cdot 37.4\,\Omega}{88\,\Omega}\right)+\left(\frac{25\,\text{cyc}\cdot(13.7\,\Omega+6.6\,\Omega)}{88\,\Omega}\right)+\left(\frac{4.5\,\text{cyc}\cdot 25.6\,\Omega}{88\,\Omega}\right)+\left(\frac{3.5\,\text{cyc}\cdot 4.7\,\Omega}{88\,\Omega}\right)}{88\,\Omega} = 324 \times 10^{-3} \qquad \text{Equation 4}$$

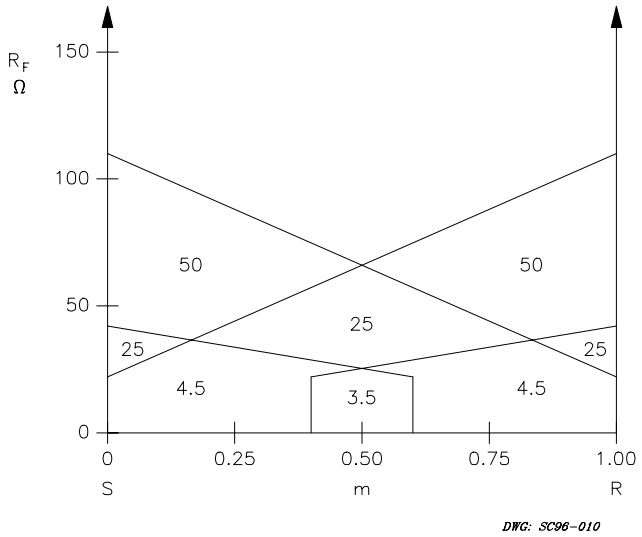

Figure 10: Fault Clearing Times (cycles) for PUTT Protection, Long Line

Permissive Overreaching Transfer Trip (POTT)

Figure 11 shows the POTT fault clearing times. Resistive faults are cleared in communication-aided time if they are detected by both Zones 2 elements. Faults that fall into a single Zone 2 are cleared sequentially in 25 cycles, assuming the local relay Zone 2 dropout time is equal to or longer than the remote relay Zone 2 pickup time.

For the long line case, the POTT figure of merit is:

$$\rho_{TR} = \frac{\left(\frac{25\text{ cyc}\cdot(37.4\,\Omega + 6.6\,\Omega)}{88\,\Omega}\right) + \left(\frac{4.5\text{ cyc}\cdot(13.7\,\Omega + 25.6\,\Omega)}{88\,\Omega}\right) + \left(\frac{3.5\text{ cyc}\cdot 4.7\,\Omega}{88\,\Omega}\right)}{88\,\Omega} = 167 \text{ x } 10^{-3} \qquad \text{Equation 5}$$

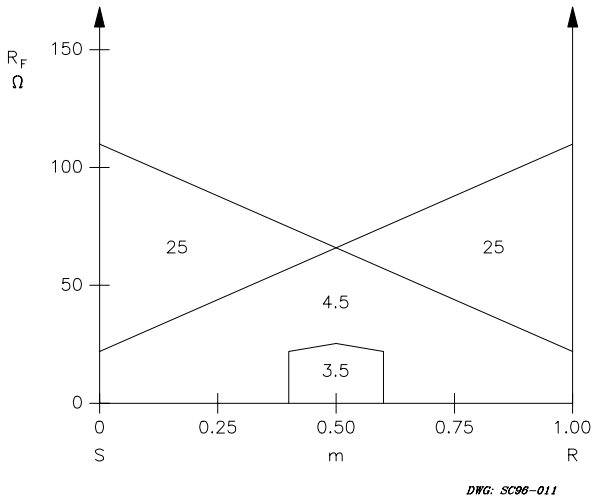

Figure 11: Fault Clearing Times (cycles) for POTT Protection, Long Line

Directional Comparison Blocking (DCB)

Figure 12 shows the DCB fault clearing times. Both ends operate and clear in 5 cycles when the fault resistance is low enough for both Zone 2 elements to operate. This is very similar to the POTT scheme. The 5-cycle time

for DCB is greater than the POTT time of 4.5 cycles because of the carrier coordination time delay that is added to the Zone 2 time in the blocking scheme.

For higher resistance faults, the DCB scheme provides faster (10 cycles) clearing than POTT schemes, because one end trips in 5 cycles, then the other end detects the fault and clears it after 5 cycles more.

For the long line case, the DCB figure of merit is:

$$\rho_{TR} = \frac{\left(\frac{10\ \text{cyc} \cdot (37.4\ \Omega + 6.6\ \Omega)}{88\ \Omega}\right) + \left(\frac{5\ \text{cyc} \cdot (13.7\ \Omega + 25.6\ \Omega)}{88\ \Omega}\right) + \left(\frac{3.5\ \text{cyc} \cdot 4.7\ \Omega}{88\ \Omega}\right)}{88\ \Omega} = 84 \times 10^{-3} \qquad \text{Equation 6}$$

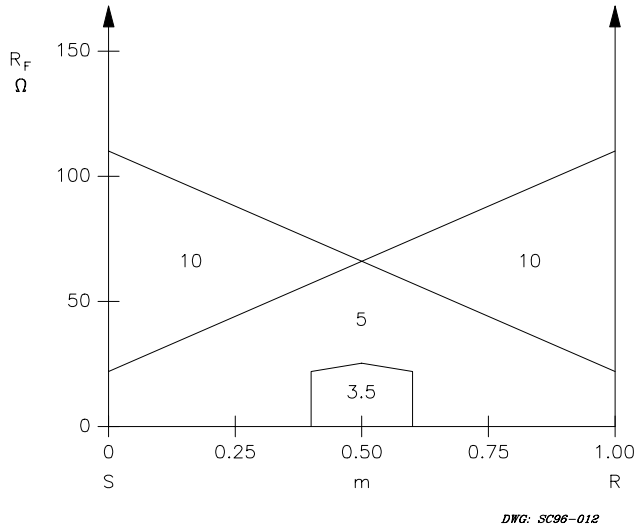

Figure 12: Fault Clearing Times (cycles) for DCB Protection, Long Line

Directional Comparison Unblocking (DCUB)

The DCUB scheme performs identically to the POTT scheme, with respect to sensitivity and operating speed, since the philosophy (trip with permission from the remote Zone 2) is the same as POTT.

Summary

Tables 6a and 6b summarize the average fault resistance coverage by high-speed tripping, average fault clearing times for all faults, and the figures of merit for each of the schemes when applied on the example long and short lines.

Table 6a: Figures of Merit and Average Fault Clearing Times for All Schemes, Long Line

	Time-Step Scheme	DUTT	PUTT	POTT	DCB	DCUB
High-Speed Rf Coverage, ohms	4.7	36.9	30.3	44	44	44
T_{ave} cyc	36.3	27.0	28.5	14.7	7.4	14.7
ρ_{TR} (x 10^3)	413	307	324	167	84	167

Table 6b: Figures of Merit and Average Fault Clearing Times for All Schemes, Short Line

	Time-Step Scheme	DUTT	PUTT	POTT	DCB	DCUB
High-Speed Rf Coverage, ohms	9.8	27.5	27.5	59.5	59.5	59.5
T_{ave} cyc	26.5	21.5	21.5	8	5.7	8
ρ_{TR} (x 10^3)	366	297	297	111	79	111

COMPLEXITY

Table 7 compares the number of protective zones and additional timers that are required by a single end of each scheme. Unless a Zone 1 element is required to implement the scheme, we did not include Zone 1 in the zone count for complexity comparison.

Table 7: Communication-Aided Protection Scheme Complexity

	POTT	PUTT	DCB	DCUB	DUTT
Basic Scheme:					
Number of Zones	1	2	2	1	1
Number of Timers	0	0	1	1	0
Current Reversal:					
Added Zones	0	0	0	0	0
Added Timers	1	0	1	1	0
Weak Infeed:					
Added Zones	1	0	N/A	1	0
Added Timers	1	0		1	0
Third Line Terminal:					
Added Timers	0	0	0	1	0
Added Logic	1	1	0	1	0
Totals:	5	3	4	7	1

A NEW COMMUNICATION-AIDED PROTECTION SCHEME

These evaluations suggested a new communication-aided protection scheme that would offer high-speed clearing of more faults while being as dependable and secure as each of the best of the existing communication schemes.

Figure 13 shows the logic for the new protection scheme. While the channel is in service, the scheme can trip three different ways:

- A fault is detected in Zone 2 for carrier coordination (CC) time if no Block Trip signal is received (traditional DCB).
- A Permissive Trip signal is received, and the fault is not behind the terminal (DCB from perspective of remote end).
- A Direct Trip signal is received (saves 0.5 cycle for lower-resistance faults).

If the channel fails (!ROK), the DCB logic (AND Gate 1) is blocked to maintain security. A 10-cycle tripping window is opened (AND Gate 2) that allows the relay to trip if a forward fault is detected. This improves dependability in instances where the channel fails as a result of the fault. A single reverse-blocking timer (RB)

disables the permissive tripping logic and extends the Block Trip signal to provide security during current reversals.

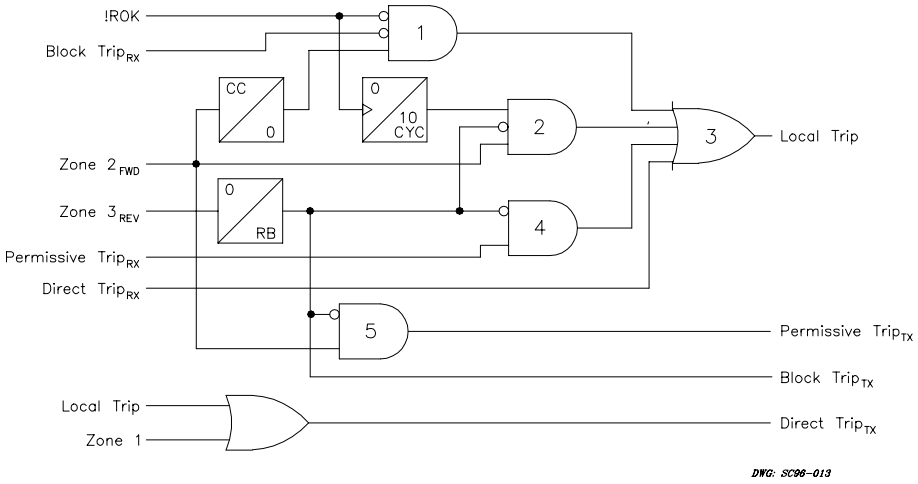

Figure 13: New Communication-Aided Tripping Logic

Dependability and security of this protection scheme are both high, with performance identical to DCUB. All faults detected at either end are cleared at both ends in 5 cycles or less. Faster clearing significantly improves the figure of merit.

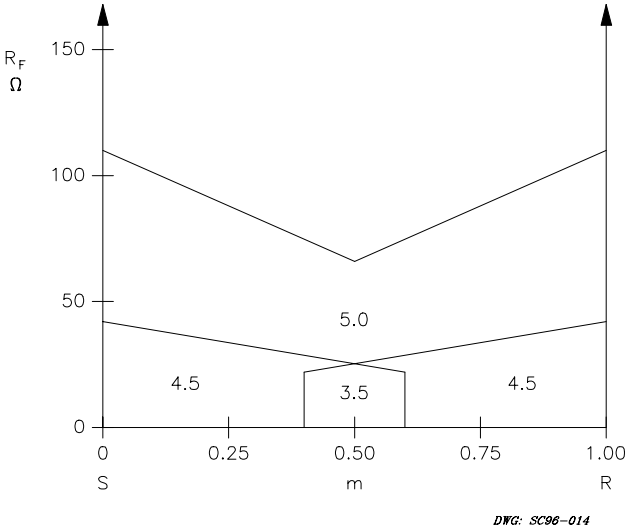

Figure 14: Fault Clearing Times (cycles) for New Protection Scheme, Long Line

$$\rho_{TR} = \frac{\left(\frac{5\,\text{cyc}\cdot(37.4\,\Omega+13.7\,\Omega)}{88\,\Omega}\right)+\left(\frac{4.5\,\text{cyc}\cdot(25.6\,\Omega+6.6\,\Omega)}{88\,\Omega}\right)+\left(\frac{3.5\,\text{cyc}\cdot 4.7\,\Omega}{88\,\Omega}\right)}{88\,\Omega} = 54 \text{ x } 10^{-3} \qquad \text{Equation 7}$$

The scheme average fault clearing time is:

$$T_{ave} = 4.74 \text{ cyc}$$

Table 8 shows the complexity figures for the new scheme. A Zone 1 element may be used to send the Direct Trip signal—thus two or three zones are used by the basic scheme. Three timers (carrier coordination, a loss-of-channel tripping window, and a reverse block timer) are used in the basic scheme, so the basic scheme is also the complete scheme.

Table 8: New Protection Scheme Complexity

Basic Scheme:	
Number of Zones	2 (3)
Number of Timers	3
Current Reversal:	
Added Zones	0
Added Timers	0
Weak Infeed:	
Added Zones	0
Added Timers	0
Third Line Terminal:	
Added Timers	0
Added Logic	0
Totals:	5 (6)

This scheme requires that three bits be communicated end-to-end. One microprocessor-based relay includes communication capabilities that make this scheme very feasible and practical.

CONCLUSIONS

Table 9 summarizes the performance of the four communication-aided protection schemes discussed above on the criteria of overtrips per year and time-delayed trips per year (assuming a 100-line system), high-speed resistive-fault coverage, total resistive fault coverage, raw and normalized figures of merit, and complexity.

The new protection scheme offers marked advantages in terms of fault resistance coverage and operating speed, with no penalty on security or dependability. Scheme complexity is comparable to POTT schemes.

Table 9: Communication-Aided Protection Performance Summary, Long Lines

	Misoperations			**Rf Coverage, Operating Time Performance**					**Complexity**
Scheme	Overtrips per year	Time-Delayed Trips per year	Figure of Merit	High-Speed Rf Coverage Ω	Total Rf Coverage Ω	Fault Clearing Time, T_{ave} Cycles	Figure of Merit ρ_{TR}	Figure of Merit, Normalized ρ_{TRN}	Zones, Timers, & Logic
POTT	0.022	12.20	12.222	44	88	14.7	167×10^{-3}	3.1	5
DCB	0.380	0.33	0.710	44	88	7.4	84×10^{-3}	1.6	4
DCUB	0.022	0.33	0.352	44	88	14.7	167×10^{-3}	3.1	7
New	0.022	0.33	0.352	88	88	4.7	54×10^{-3}	1.0	5 (6)

Assumptions: Long Line, 1% probability of channel loss during a fault

APPENDIX A: PROTECTION SCHEME LOGIC

DIRECT UNDERREACHING TRANSFER TRIP (DUTT)

The DUTT scheme uses an instantaneous Zone 1 element to trip the local circuit breaker and initiate a transfer trip to the remote end. The remote end trips immediately on receipt of the transfer trip signal, without any additional qualification. This scheme is extremely simple but is susceptible to misoperation if channel noise keys the Direct Trip signal.

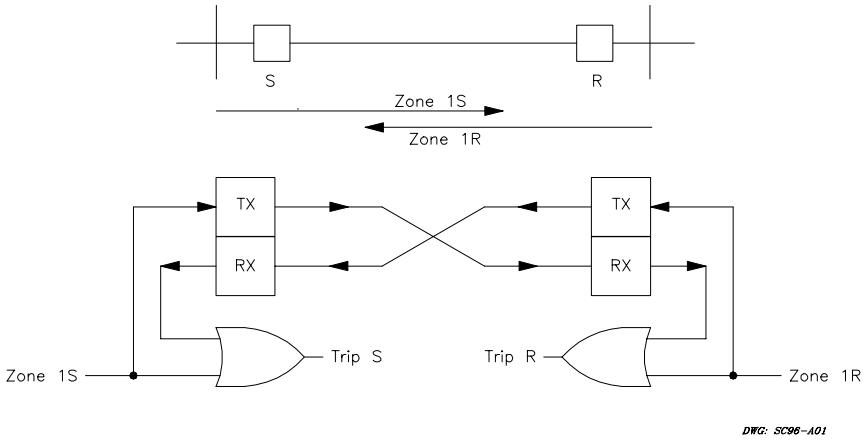

Figure A1: Direct Underreaching Transfer Trip (DUTT) Logic

PERMISSIVE UNDERREACHING TRANSFER TRIP (PUTT)

The PUTT scheme uses Zone 1 to trip the local breaker and send a permissive trip signal to the remote end. The remote end breaker trips when it receives the permissive signal, if its Zone 2 element is detecting a fault. By using the Zone 2 element to supervise tripping on receipt of the permissive signal, this scheme is less susceptible to misoperation under noisy channel conditions than the DUTT scheme, above. Because the scheme uses an underreaching element to send permission, PUTT does not send a permissive signal for out-of-section faults. PUTT schemes do not require additional supervisory logic to maintain security under current reversal conditions on parallel lines.

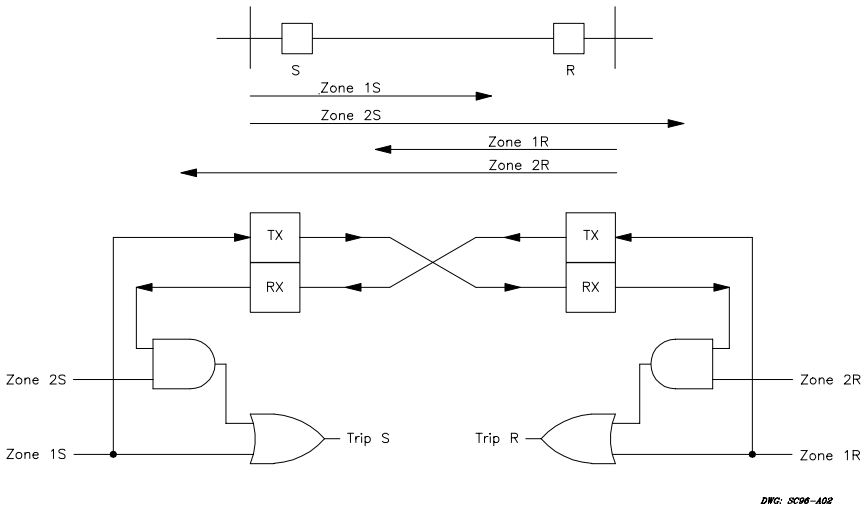

Figure A2: Permissive Underreaching Transfer Trip (PUTT) Logic

PERMISSIVE OVERREACHING TRANSFER TRIP (POTT)

POTT schemes use an overreaching Zone 2 element to send a permissive trip signal to the remote end. The remote end breaker trips when it receives the permissive signal, if its Zone 2 element is detecting a fault. Because the scheme uses an overreaching element to send permission, POTT schemes need additional supervisory logic to maintain security under current reversal conditions on parallel lines.

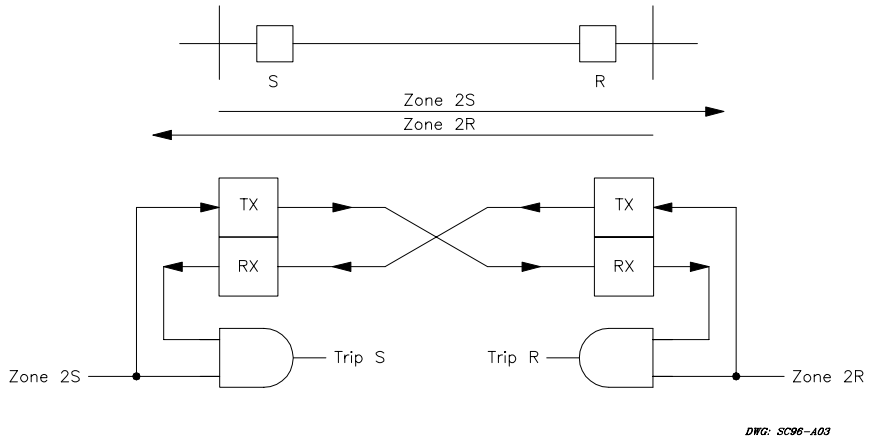

Figure A3: Permissive Overreaching Transfer Trip (POTT) Logic

DIRECTIONAL COMPARISON BLOCKING (DCB)

Unlike the schemes described above, which send a signal when a fault is detected in the forward direction, DCB schemes send a signal (Block Trip) when a fault is detected in the reverse direction.

If the local relay detects a reverse fault, it sends a Block Trip signal to the remote end. At the remote end, the overreaching Zone 2 elements are allowed to trip, following a short coordinating time delay, if they are not blocked by the arrival of the Block Trip signal. In many applications, a nondirectional element is used to send the Block Trip signal. In these cases, the block signal is quickly shut off if the fault is in the forward direction.

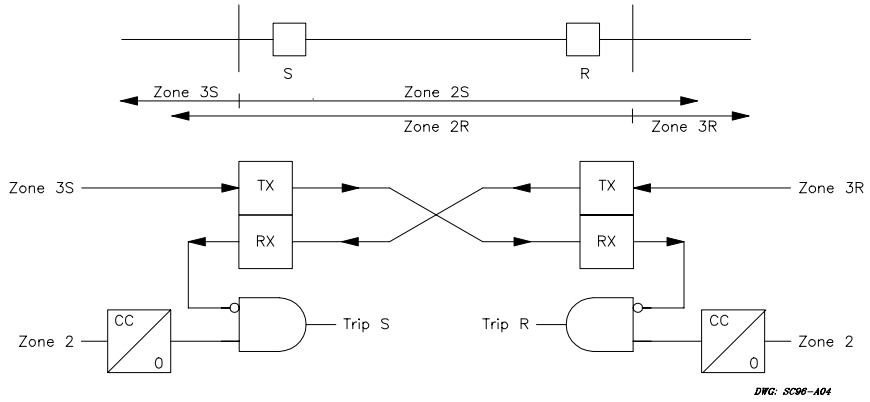

Figure A4: Directional Comparison Blocking (DCB) Logic

DIRECTIONAL COMPARISON UNBLOCKING (DCUB)

In DCUB schemes, a guard signal is continuously sent between the two ends of the transmission line. If a fault is detected by the local relay Zone 2 element, the guard signal is shut off and a trip signal is sent. The remote relay detects the change in signals from guard to trip. If it also detects a fault in Zone 2, it trips. DCUB schemes also

use logic that permits a trip if a loss-of-guard is detected and a fault in Zone 2 is also detected, even if a trip signal is not received.

APPENDIX B : MARKOV RELIABILITY MODELS

Three Markov models were developed for the security and dependability comparisons. Results from models of a POTT, DCB, and DCUB scheme were compared. We assumed that ideal time-stepped backup protective relays were applied with each primary communication-aided tripping scheme, so that a fault would never be present on the system longer than Zone 2 tripping time. We further assumed that every trip resulted in a successful reclose. With some added complexity, the models could be modified to account for unsuccessful recloses. Table B2 lists the remaining performance assumptions. Figures B1, B2, and B3 illustrate the POTT, DCB, and DCUB models and their resulting calculation matrices.

Table B1: Markov Model Variables

Variable	Value Used	Description
MTBF	75 years	Protection Mean Time Between Failures (2 relays, 150 year MTBF each)
ST	0.80	Relay Self-Test Effectiveness
MTBFc	50 years	Channel Equipment MTBF
Fcf	1.0% 0.1%	Additional Channel Failures Due to Faults
MTRT	2 hours	Mean Time to Test Relay
MTTR	4 hours	Mean Time to Repair Relay or Channel Equipment
MTT79	35 cycles	Longest Reclosing Open Interval, plus Breaker Time
MTTTc	5 cycles	Communication-Aided Fault Clearing Time
Z2D	24 cycles	Zone 2 Fault Clearing Time
Z1D	3.5 cycles	Zone 1 Fault Clearing Time
kz	0.01%	Percent of External Faults That Cause Communication Channel Misoperation

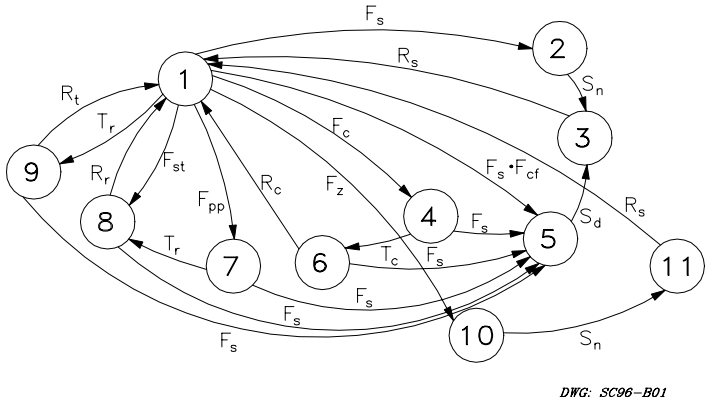

Figure B1: POTT Markov Model

State 1 of this Markov model represents the normal operating condition of the power system and protection: the protected line is energized, the relay is in service, and the communication channel is operating properly. When a system fault occurs, the system moves to State 2. Communication-aided tripping takes the system to State 3, and reclosing restores the system to State 1. These are the normal and preferred transitions.

States 7, 8, and 9 have the primary protective relays out of service due to an undetected failure (State 7), a detected failure (State 8), or a routine test (State 9). If a fault occurs while the system is in one of these states, time-delayed backup protection clears the fault (State 5), and reclosing restores the system. An assumption is made that a time-delayed fault clearance will result in a check on the substation that will cause the relays to be quickly placed back into service.

If a fault occurs while the communication channel is out of service due to failure or repair (States 4 and 6), the system moves to State 5, where time-delayed fault clearing and reclosing restore the system.

The Markov model accounts for a small percentage of in-section faults that can cause the communication channel to fail, resulting in a time-delayed trip. These are represented by the direct transition from State 1 to State 5. In a POTT scheme, we assume that there is a yet smaller percentage (kz = 0.01%) of communication channel failures during detected external faults that can result in a permissive trip signal being erroneously received by a relay. This would result in an overtrip misoperation and reclose, represented by States 10 and 11. The probabilities of interest are P_5, representing time-delayed trip misoperations, and $P_{10} + P_{11}$, representing overtrip misoperations. The model transition rates are defined in terms of operations per hour, then the matrix, T, below is used to calculate the individual probabilities.

$$
T = \begin{bmatrix}
a11 & Fs & 0 & Fc & Ff & 0 & Fpp & Fst & Tr & Fz & 0 \\
0 & a22 & Sn & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
Rs & 0 & a33 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & a44 & Fs & Tc & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & Sd & 0 & a55 & 0 & 0 & 0 & 0 & 0 & 0 \\
Rc & 0 & 0 & 0 & Fs & a66 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & Fs & 0 & a77 & Tr & 0 & 0 & 0 \\
Rr & 0 & 0 & 0 & Fs & 0 & 0 & a88 & 0 & 0 & 0 \\
Rt & 0 & 0 & 0 & Fs & 0 & 0 & 0 & a99 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & aaa & Sn \\
Rs & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & abb
\end{bmatrix}
$$

a11=1-(Fs+Fc+Ff+Fst+Fpp+Tr+Fz)
a22=1-Sn
a33=1-Rs
a44=1-(Fs+Tc)
a55=1-Sd
a66=1-(Rc+Fs)
a77=1-(Fs+Tr)
a88=1-(Fs+Rr)
a99=1-(Fs+Rt)
aaa=1-Sn
abb=1-Rs

$P^T = [P_1\ P_2\ P_3\ P_4\ P_5\ P_6\ P_7\ P_8\ P_9\ P_{10}\ P_{11}]$
$P^T * T = P^T$ or $P^T * [T - 1] = 0$

Where I = Identity Matrix
and $_i\Sigma P_i = 1$

InDep = P(5)
InSec = P(10)+P(11)

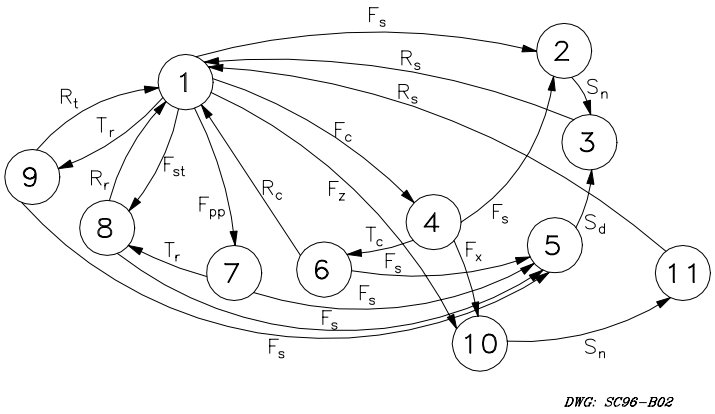

Figure B2: DCB Markov Model

The DCB scheme Markov model differs from the POTT model in how the system responds to faults that occur while the channel is out of service. In-section faults are cleared in normal communication-aided time, as soon as the relay's carrier coordination timers expire (transition from State 4 to State 2). An overtrip misoperation occurs (State 10) if a detected out-of-section fault occurs while the channel is down. As with the POTT scheme, a very small percentage of external faults also generate misoperations when the blocking signal fails to reach the remote relay (direct transition from State 1 to State 10). The Markov matrix and calculations for the DCB scheme are shown below.

$$
T = \begin{bmatrix}
a11 & Fs & 0 & Fc & 0 & 0 & Fpp & Fst & Tr & Fz & 0 \\
0 & a22 & Sn & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
Rs & 0 & a33 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & Fs & 0 & a44 & 0 & Tc & 0 & 0 & 0 & Fx & 0 \\
0 & 0 & Sd & 0 & a55 & 0 & 0 & 0 & 0 & 0 & 0 \\
Rc & 0 & 0 & 0 & Fs & a66 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & Fs & 0 & a77 & Tr & 0 & 0 & 0 \\
Rr & 0 & 0 & 0 & Fs & 0 & 0 & a88 & 0 & 0 & 0 \\
Rt & 0 & 0 & 0 & Fs & 0 & 0 & 0 & a99 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & aaa & Sn \\
Rs & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & abb
\end{bmatrix}
$$

$$a11 = 1 - (Fs + Fc + Fst + Fpp + Tr + Fz)$$
$$a22 = 1 - Sn$$
$$a33 = 1 - Rs$$
$$a44 = 1 - (Fx + Fs + Tc)$$
$$a55 = 1 - Sd$$
$$a66 = 1 - (Rc)$$
$$a77 = 1 - (Fs + Tr)$$
$$a88 = 1 - (Fs + Rr)$$
$$a99 = 1 - (Fs + Rt)$$
$$aaa = 1 - Sn$$
$$abb = 1 - Rs$$

$$P^T = [P_1\ P_2\ P_3\ P_4\ P_5\ P_6\ P_7\ P_8\ P_9\ P_{10}\ P_{11}]$$
$$P^T * T = P^T \text{ or } P^T * [T - 1] = 0$$

Where I = Identity Matrix
and $_i\Sigma P_i = 1$

$$InDep = P(5)$$
$$InSec = P(10) + P(11)$$

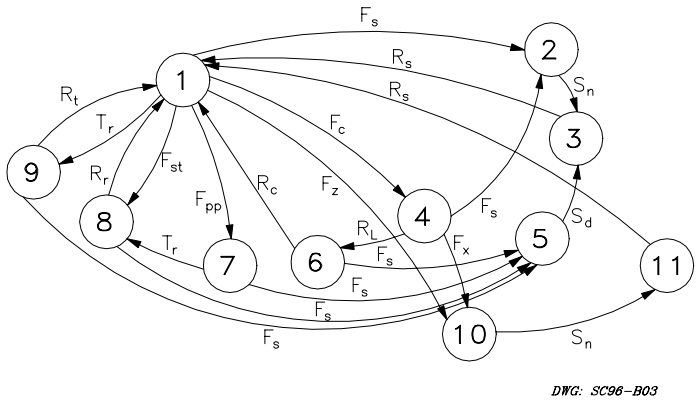

Figure B3: DCUB Markov Model

The Markov Model for the DCUB scheme is also similar to the POTT model, but accounts for the 150 ms tripping window that is opened on loss-of-guard using State 4. Internal and detected external faults are both cleared quickly (State 2 or State 10) if they occur while the system is in State 4. We assume that a sustained loss-of-guard will generate an alarm, allowing the channel equipment to be repaired, taking the system from State 6 to State 1.

```
          a11 Fs  0   Fc  0   0   Fpp Fst Tr  Fz  0
          0   a22 Sn  0   0   0   0   0   0   0   0
          Rs  0   a33 0   0   0   0   0   0   0   0
          0   Fs  0   a44 0   Rl  0   0   0   Fx  0
          0   0   Sd  0   a55 0   0   0   0   0   0
          Rc  0   0   0   Fs  a66 0   0   0   0   0
T =       0   0   0   0   Fs  0   a77 Tr  0   0   0
          Rr  0   0   0   Fs  0   0   a88 0   0   0
          Rt  0   0   0   Fs  0   0   0   a99 0   0
          0   0   0   0   0   0   0   0   0   aaa Sn
          Rs  0   0   0   0   0   0   0   0   0   abb
```

```
  a11=1-(Fs+Fc+Fst+Fpp+Tr+Fz)
  a22=1-Sn
  a33=1-Rs
  a44=1-(Fs+Rl+Fx)
  a55=1-Sd
  a66=1-(Rc+Fs)
  a77=1-(Fs+Tr)
  a88=1-(Fs+Rr)
  a99=1-(Fs+Rt)
  aaa=1-Sn
  abb=1-Rs
```

$P^T = [P_1\ P_2\ P_3\ P_4\ P_5\ P_6\ P_7\ P_8\ P_9\ P_{10}\ P_{11}]$

$P^T * T = P^T$ or $P^T * [T - 1] = 0$

Where I = Identity Matrix

and $_i\Sigma P_i = 1$

```
  InDep=P(5);
  InSec(k)=P(10)+P(11)
```