Real-Time Power System Control Using Synchrophasors

Edmund O. Schweitzer, III and David E. Whitehead
Schweitzer Engineering Laboratories, Inc.

Presented at the
62nd Annual Georgia Tech Protective Relaying Conference
Atlanta, Georgia
May 21–23, 2008

Previously presented at the
61st Annual Conference for Protective Relay Engineers, April 2008,
and 7th Annual Clemson University Power Systems Conference, March 2008,

Also presented at the
DistribuTECH Conference, January 2008, under the title
"Real-Time Synchrophasor Control"

Originally presented at the
34th Annual Western Protective Relay Conference, October 2007

Real-Time Power System Control Using Synchrophasors

Edmund O. Schweitzer, III and David E. Whitehead, *Schweitzer Engineering Laboratories, Inc.*

***Abstract*—To date, synchronized phasor measurements have been used mainly for power system model validation, postevent analysis, real-time display, and other similar activities. However, synchrophasors have a greater potential than monitoring and visualization. Synchrophasors will increasingly contribute to the reliable and economical operation of power systems as real-time control and protection schemes become broadly used. Synchronous phasor measurements are now available in relays and meters; however, a practical means of processing the data in real time had been lacking.**

This paper describes a synchronous vector processor and several practical applications, including automated diagnostics, remedial action schemes, direct state measurement, and stability assessment.

I. Introduction

Synchronous phasor measurements come from dedicated phasor measurement units (PMUs), and more recently from protective relays and meters. Originally, the measurements were mainly available in streaming messages, per the IEEE Standard C37.118 [1]. Meters and relays today also make the measurements available in other protocols and methods, so the data can be easily used by SCADA and real-time control systems. Some information processors can package the information into protocols, like DNP3, and some relays can package the information into IEC 61850 objects.

The streaming data per C37.118 have been collected in Phasor Data Concentrators (PDC) [2], [3], but these concentrators cannot truly process the data using algorithms, nor can they effect control. Nevertheless, concentrated data have been put to work to:

- Monitor power flows
- Analyze wide-area power system events
- Improve state estimation models
- Archive system performance

Most systems described in the literature involve off-line processing or relatively slow processing. Reference [4] suggests a substation SuperCalibrator where "the data from each IED is collected in a COMTRADE format and processed into providing data sets in time instances, t1, t2, etc. In the future this process will be fully automated." It describes how such a device might be used for improving data supplied to state estimators, but never discusses the details of such a device.

There is a compelling need for a processing device that receives synchronous phasor measurements from one or more relays, meters, or PMUs; time-aligns these data to near exactness; performs vector mathematics; executes programmable logic; and sends commands to relays or other fast-acting devices within time periods short enough to be perceived as real time. Given that the data can be received every cycle, the processing device should be able to update every cycle, when needed.

This paper describes a user-programmable, real-time synchrophasor processor and a few of its applications. To emphasize its ability to perform vector mathematics in real time, we have chosen to call the device a Synchrophasor Vector Processor.

II. The Synchrophasor Vector Processor

The purpose of the Synchrophasor Vector Processor (SVP) is to collect synchronous phasor measurements (SPMs), collect logical inputs, perform vector and scalar calculations, make decisions, produce outputs, and report data. A simple task for an SVP might be collecting SPMs from two ends of a transmission line, comparing the voltage angles, and issuing a warning to an operator if a threshold has been exceeded. A more complicated example might be distributed SVPs performing localized substate measurement and forwarding results to a higher level, to build the entire state vector, in real time, and without the nonlinear and time-consuming steps of state estimation.

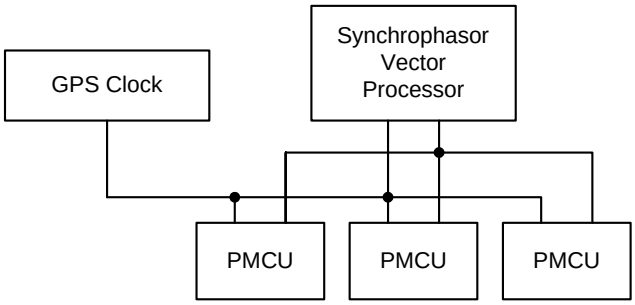

Fig. 1. Real-Time Synchrophasor Control System

Fig. 1 shows the components of a real-time synchrophasor control system. It consists of:

- *Microsecond-Accurate Clock, Like a GPS Clock.* Because time is the reference point for a synchrophasor system it is important to use a high-quality clock. Microsecond-accurate clocks are fairly commonplace, inexpensive, and in many substations. As we begin to rely on microsecond timing, we must design reliable timing means and be prepared for the instances when the time sources may fail. For instance, on December 6, 2006, a very strong solar flare disrupted GPS services in daylight regions of the world for up to ten minutes [5]. Fortunately, today's clocks signal the accuracy of their timing, and

we can use this information to modify or even disable logic when accurate timing is unavailable. When synchronous phasor measurement processing is limited to a single substation, the absolute reference in time is not important; however, the *relative* timing of all devices at that station remains important, but independent of satellites. One electrical degree at 60 Hz is 46.29 microseconds, so timing errors up to approximately 10 microseconds can be tolerated. Reference [6] is a practical treatment of time sources and system errors, explaining how to design quality timing systems.

- *Phasor Measurement and Control Units (PMCUs)* [7]. These may be dedicated devices, as well as relays or meters and other equipment that provide the synchronous measurements. Sending synchronous measurements is the key requirement for the phasor measurement device. The most common synchrophasor format is IEEE C37.118. Other formats exist that may be suitable for certain applications and provide opportunities for new communications methods. The PMCU must time-align its measured quantities to the common time reference. In order for a synchrophasor control system to perform control, the PMCU must be capable of receiving control commands, or separate control devices must be added. IEEE C37.118 does not specifically accommodate control commands. Therefore, the PMCU must be capable of control via some other protocol like DNP3, IEC 61850, SEL MIRRORED BITS® communications, or SEL Fast Message.
- *Communications Channels.* Specific applications dictate the communications requirements. These range from one message a minute to one per cycle. For some applications, serial communications at 9600 bps will work. For high-speed applications where large amounts of synchrophasor data are transmitted, an Ethernet or similar communications channel may be required.
- *The Synchrophasor Vector Processor*. The SVP collects, time-aligns, performs control operations/algorithms on the data, and then issues command/signals and shares data. In order to ensure that the fastest received SPM can be processed before the next one is received, the SVP must be capable of completing its control loop processing at least every cycle.

The SVP is a computer rated for utility applications, with specialized I/O and processing capabilities. The SVP is designed to preserve microsecond timing throughout and to perform vector and matrix mathematics at high speed and efficiency. The rear panel of an SVP is shown in Fig. 2.

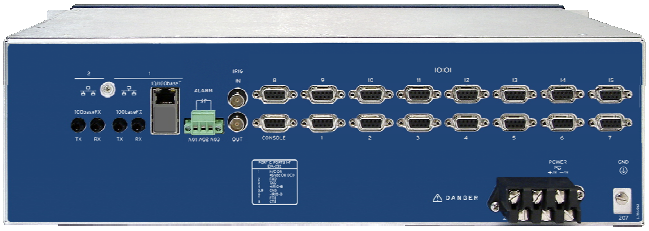

Fig. 2. Synchrophasor Vector Processor Connections

This implementation consists of: a 1.1 GHz processor, 512 kB of RAM, and 1 GB Flash memory. An optional hard drive is available for local synchrophasor data archiving. Because hard drives are typically not substation-hardened, as an alternative, the SVP can forward the synchrophasor data to a remote archive location. The operating system and application firmware have been minimized for efficiency, security, and reliability. Email, web browser, and other nonessential programs have been removed from the SVP operating system package because they are not required to perform vector-processing functions. We implemented a soft-core programmable logic controller based on IEC 61131-3 [8] that includes powerful and efficient functions for vector and complex math. IEC 61131-3 defines six different programming methods. Generally, we use two of the six: functional block diagrams and Structured Text. Fig. 3 shows a functional block diagram example that graphically describes digital and analog expressions.

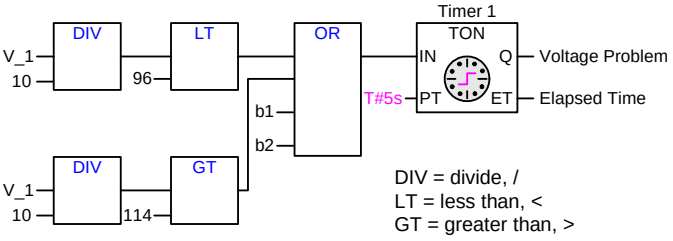

Fig. 3. IEC 61131-3 Functional Block Diagram

Fig. 4 is an example of Structured Text programming language. Structured Text allows advanced users to program the SVP in a language similar to C and Pascal, using statements like IF, WHILE, CASE, and FOR. Structured Text is ideal for conditional programming, loops, and other similar complex program flow routines.

```
UsePointer (PRG-ST)
0001 PROGRAM UsePointer
0002 VAR
0003     ppAType      : POINTER TO POINTER TO TypeWithPointer;
0004     pAType       : POINTER TO TypeWithPointer;
0005     ATypeInst1   : TypeWithPointer;
0006     ATypeInst2   : TypeWithPointer;
0007     aiBuffer     : ARRAY[0..5] OF INT := 1000,2000,3000,4000,5000,6000;
0008     n            : INT(0..5) := 3;
0009     Timer        : TON;
0010 END_VAR
0011 VAR_OUTPUT

0001 ATypeInst1.piVal := ADR(aiBuffer[0]);
0002 ATypeInst2.piVal := ADR(aiBuffer[n]);
0003
0004 pAType := ADR(ATypeInst1);
0005 ppAType := ADR(pAType);
0006
0007 pAType := ADR(ATypeInst2);
0008
0009
0010 Timer(IN:= FALSE, PT := t#25s, Q => bBool);
0011
```

Fig. 4. IEC 61131-3 Structured Text Example

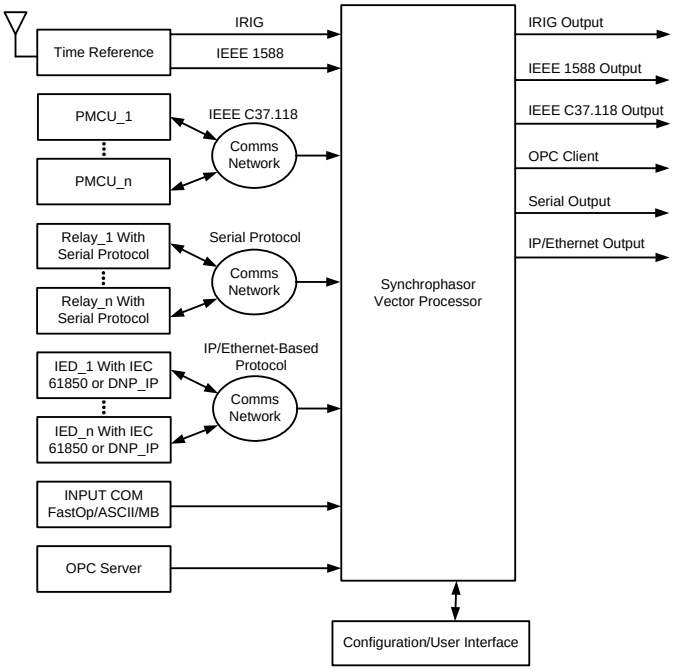

Fig. 5. SVP Input/Output Block Diagram

Fig. 5 shows the inputs and outputs of an SVP. The I/O attributes of the SVP include the following:

- *Time Reference Input.* For precision, the SVP accepts accurate time with a resolution and accuracy of one microsecond or better. IRIG-B time code from a suitable clock fulfills this requirement. Other time schemes sometimes used in real-time systems include Network Time Protocol (NTP), Simple Network Time Protocol (SNTP), DNP3 timestamps, etc., but microsecond accuracy is not achieved. IEEE Standard 1588–2002 [9] promises submicrosecond synchronization of real-time clocks, but this technology is not broadly available today. The SVP provides a time quality indication so the user knows what time source is being used in calculations and if it meets synchronized phasor accuracies. A time source is used to timestamp all data inputs, to provide an accurate clock source to the logic engine, and to timestamp output data (if required).
- *IEEE C37.118 Input.* IEEE C37.118 is a standard for synchronized phasor measurement systems in power systems. IEEE C37.118 is not media dependent. It can be used on EIA-232 and Ethernet communications connections. It addresses the definitions of synchronized phasor, time synchronization, application of timetags, method to verify measurement compliance with the standard, and message formats for communication with PMCUs. These data are the most accurate today.
- *Serial Protocol Input.* These messages are received via serial links typically 115 kbps or slower using EIA-232 or EIA-485 communications links. These protocols include DNP3, Modbus® RTU, CANbus, SEL Fast Message, etc.
- *Ethernet Protocol Input.* These messages are from devices with IEC 61850, DNP3 LAN/WAN, Modbus/TCP, Telnet, etc. Ethernet provides faster speed (10/100 Mbps) and multiple logical connections for each physical connection.
- *Input Controls.* These inputs can be from proprietary data formats like SEL Fast Message, SEL Remote Bits, SEL MIRRORED BITS communications, etc.
- *OPC Server Input.* The SVP OPC can request data from an external OPC Server. The data can then be used internally with other data inputs e.g., C37.118.
- *Configuration Port.* A user configuration port allows users to set, modify, monitor, and otherwise configure the SVP.
- *IP/Ethernet Output*. This output stream is generated by the logic and control functions of the SVP. The output protocols include IEC 61850, DNP3 LAN/WAN, Modbus/TCP, etc.
- *Serial Output.* This output stream is generated by the logic or control functions of the SVP. The protocols include SEL Fast Message, DNP3, Modbus RTU, CANbus, SEL MIRRORED BITS communications, etc.
- *OPC Client Output.* An internal OPC Server provides data to external OPC Client requests.
- *IEEE C37.118 Output.* This port can output a data stream assembled by the SVP from multiple received C37.118 packets. It is similar to the output of synchrophasor data concentrators.

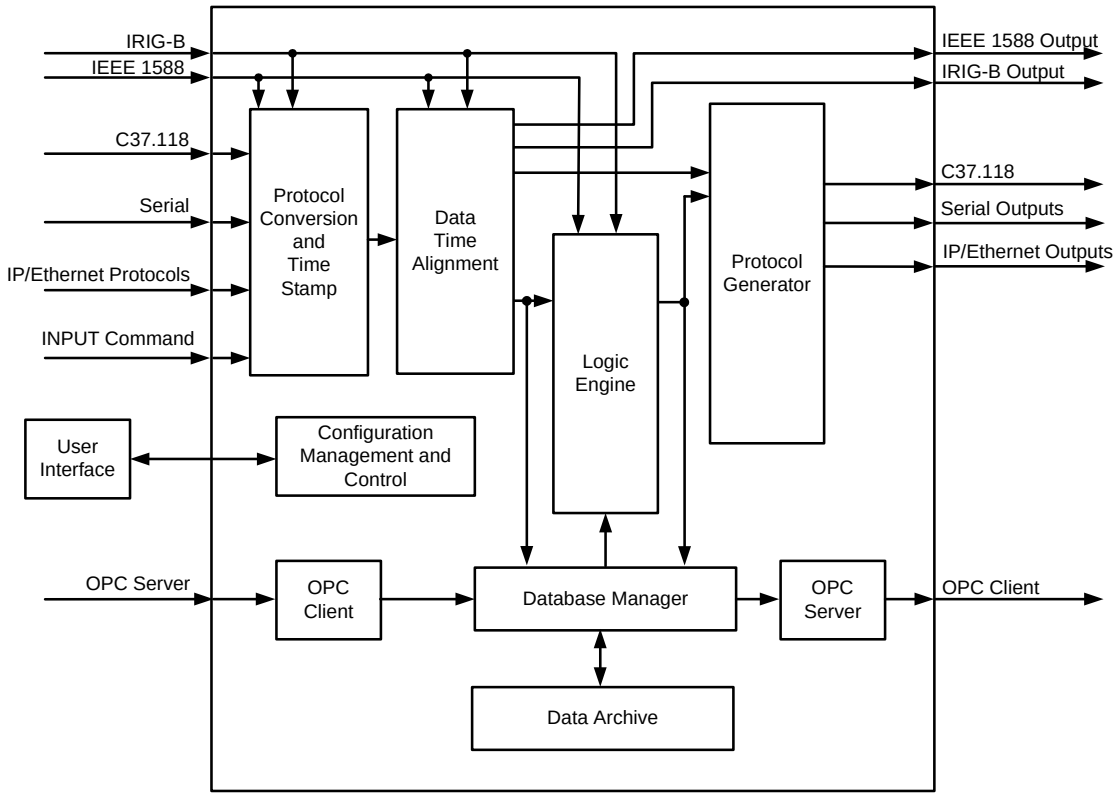

Fig. 6. SVP Functional Block Diagram

Fig. 6 shows the SVP internal functional block diagram. The major SVP functional blocks are as follows:

- *Protocol Conversion and Timestamp.* This block translates IEEE C37.118, serial data, IP/Ethernet protocols, and input commands into a common data format/structure. For protocols that do not support time information, a timestamp for the data is added. Examples of protocols that do not have time information are Modbus, and SEL Fast Message. IEEE protocols such as C37.118, IEC 61850, and SEL Synchrophasor Fast Message already have a timestamp.
- *Data Time Alignment*. Data may be measured at the same time but delayed during communication. The Data Time Alignment block correlates data blocks based on time to compensate for unequal communications delays.
- *Logic Engine.* The Logic Engine is a soft-core programmable logic controller (PLC) with vector and complex math capabilities. Data inputs to the Logic Engine are from the Data Time Alignment block. The Logic Engine can also access the Database Manager to retrieve stored data, as required for logic processing.
- *Protocol Generator*. Outputs from the Logic Engine are sent to the Protocol Generator. It converts the results into appropriate protocols such as IEEE C37.118, DNP3 LAN/WAN, Modbus RTU, SEL MIRRORED BITS communications, SEL Fast Message, etc.
- *Database Manager*. The Database Manager interfaces to the Data Time Alignment block and the output of the Logic Engine. The Database Manager formats data for storage, performs the OPC Client query, and provides OPC Server responses. It also provides data to the Logic Engine for use in control algorithms.
- *OPC Client*. The OPC Client performs OPC requests for data as defined by user setting or the Logic Engine.
- *OPC Server*. The OPC Server serves data to external OPC clients. The data may be raw data from the Data Time Alignment block, Logic Engine, or Data Archive block.
- *Configuration Manager and Control (CMC).* The CMC provides a user interface to configure the various communications inputs, Logic Engine algorithms, communications output format configurations, database management, and other various configuration duties.

III. PROCESSING CAPABILITIES

The purpose of the SVP is to perform complex vector math fast enough to control power system activity. As mentioned earlier, the processing interval can be as short as one cycle. How much processing can the SVP do in one cycle?

Consider this “heavy-duty” processing scenario:

- SVP processing interval: 4 milliseconds.
- Number of connected PMCUs: 16, where each is sending 12 phasor measurements, 8 analog quantities, and 32 digital points.
- Data input: Once a cycle, 16.667 milliseconds
- Control command output interval: 4 milliseconds.

Design, analysis, and testing have shown that approximately 50 percent of the CPU resources are used by the

operating system and synchrophasor data formatting. This leaves approximately 50 percent of the CPU resources to implement user-defined control logic. Putting the 50 percent CPU control logic application into perspective, the RAS scheme described in Section V uses approximately 5 percent of the CPU. This processing power is sufficient for a broad range of applications.

IV. Monitoring and Warning System

Fig. 7 depicts a two-bus, parallel transmission line system. A PMCU performs protection and synchrophasor functions at each end of the transmission lines. An SVP is located at each bus. The SVP collects synchrophasor data from each PMCU and monitors the quality of the bus voltage measurements.

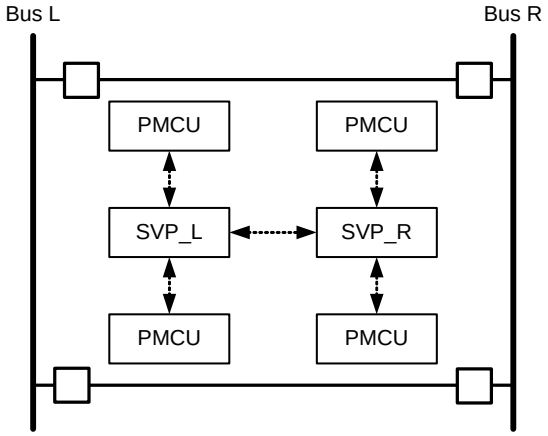

Fig. 7. Transmission System

When the breakers are closed, the line voltages at each bus should agree in magnitude and phase. For example, at Bus L, SVP_L collects synchrophasor data from each PMCU and computes an alarm condition if the voltage difference or angle difference is greater than 1 percent for 10 seconds using the following logic:

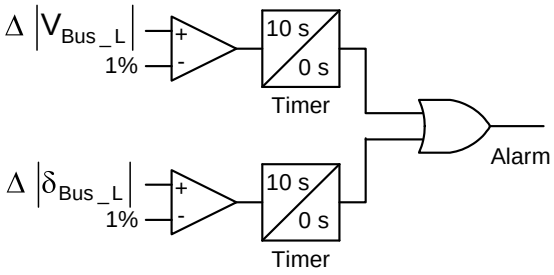

Fig. 8. Bus Voltage Monitor

Using a similar configuration at the remote bus, Bus R, SVP_R performs the same monitoring function. An advantage of the SVP system shown above is that two SVPs can exchange synchrophasor data. This capability allows for an additional measurement quality check at Bus L. Using line parameter information and voltage and current synchrophasor data from Bus R, we can calculate the voltage at Bus L using (1):

$$V_{Bus\_L} = V_{Bus\_R} + Z \cdot I_{Bus\_R} \quad (1)$$

With this result we can compare the calculated values with the measured values. Using similar logic to that described above, an alarm can be generated for an out-of-tolerance deviation. What is interesting is a new ability (not possible before synchrophasors) to provide various overlapping checks, using the SVP, to notify operators of potential problems.

V. Remedial Action Scheme (RAS)

Compare a traditionally implemented RAS system and one implemented using an SVP approach. Assume that in both cases the line relays can transmit synchrophasor information and receive digital control commands, i.e., they are PMCUs.

The system under consideration consists of three 345 kV and two 230 kV transmission lines, four generators, and various switches and circuit breakers. Fig. 9 shows the one-line diagram of the system.

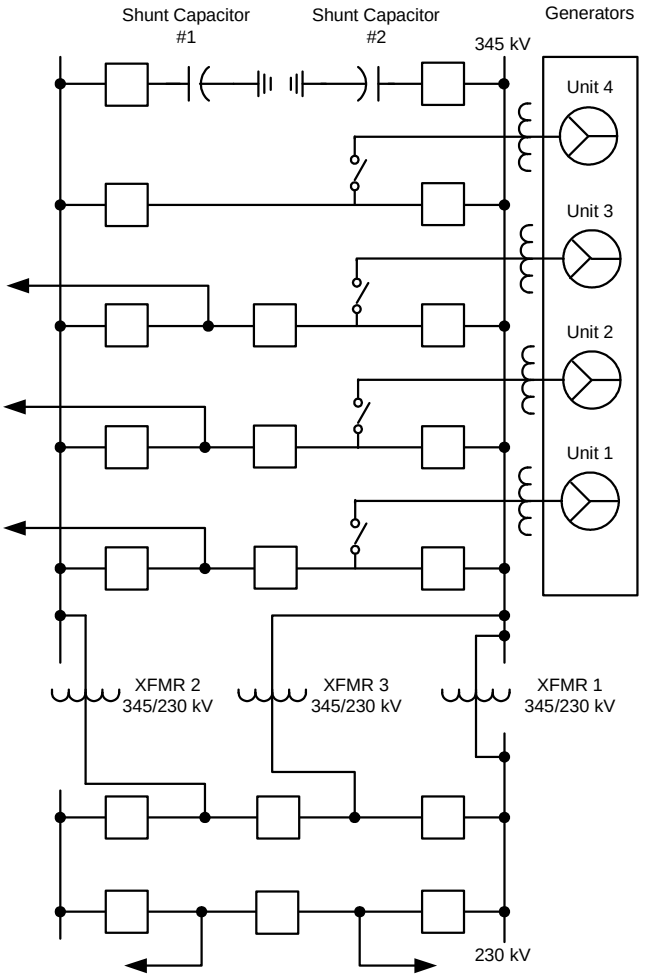

Fig. 9. Power System for RAS

The RAS takes action for an event that causes system instability e.g., loss of one or more lines by dropping generation. To avoid system instability, the generation must be dropped within five cycles of an event that could cause instability. The timing budget for removing generation is as follows:

- One cycle for RAS controller detection and decision
- One cycle for the breaker relay output detection time
- Three cycles for the breaker operation clearing time

For security/reliability purposes a triple-double redundant RAS was developed with a two out of three voting scheme.

A. Traditional RAS Scheme Implementation

Traditional relays monitor each transmission. In an abnormal condition, the relay asserts a contact that is monitored by three separate I/O modules. Each I/O module passes the status to its respective logic processor. Each logic processor calculates which generator to shed. The logic processors then transfer their decision to the other logic processors. The logic processors compare the received decisions with their own. If two of the three decisions are to trip, a trip command is issued through the I/O modules to the generator relays. Fig. 10 shows the timing diagram of these events. Included are the relay detection time and relay assertion output time. The system consists of approximately 73 individual pieces of equipment, including I/O modules and logic processors.

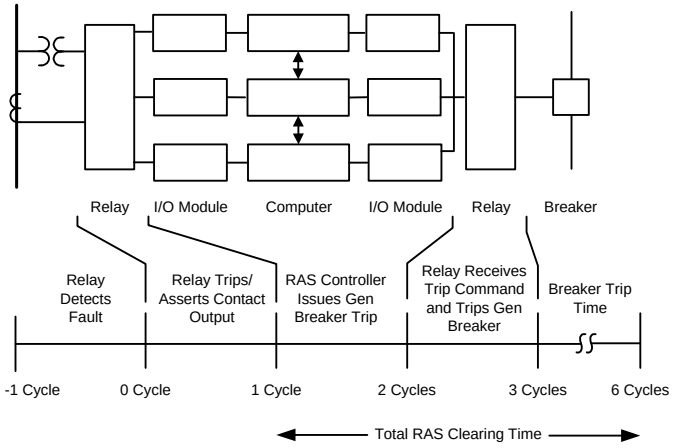

Fig. 10. RAS Clearing Time Budget

B. SVP Implementation

Because we are using synchrophasors, we can take analog quantities directly from the relays instead of the post-processed trip outputs from the relays. For our SVP RAS implementation, the relays forward synchrophasor data, and the SVP determines if there is a loss of load, over-power, etc. For the SVP RAS scheme, we have the following timing allocations:

- One cycle for the SVP RAS controller detection and decision
- One-quarter cycle to trip the PMCU
- Three cycles for the breaker operation clearing time

The net result is implementing an SVP solution and using high-speed communications tripping can save three quarters of a cycle.

Fig. 11 shows the SVP RAS clearing timing and Fig. 12 shows a lab test configuration.

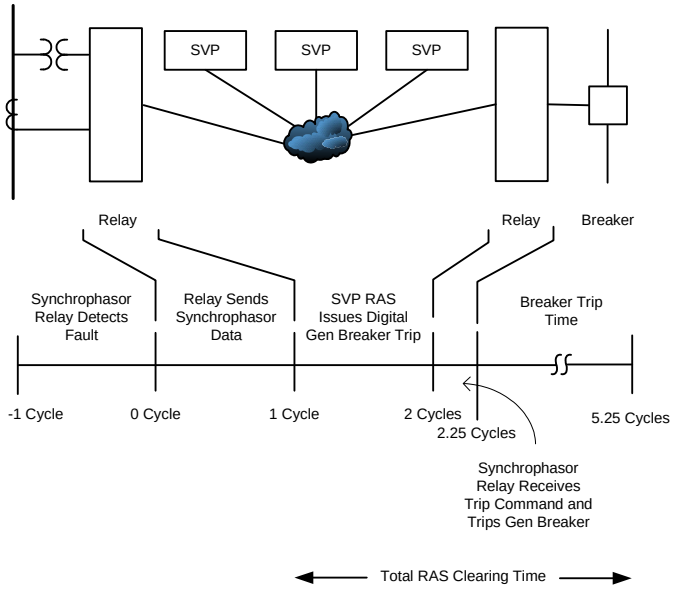

Fig. 11. SVP RAS Clearing Time

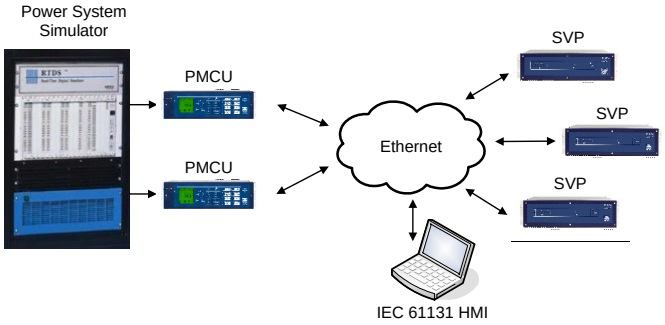

Fig. 12. SVP RAS Lab Test Configuration

There are other advantages to the SVP RAS approach, including reduced equipment count, reduced wiring, reduced complexity, reduced power supply requirements, greater scheme flexibility, and improved MTBF. Table I compares the two solutions.

TABLE I
TRADITIONAL VS. SVP RAS SCHEME COMPARISON

	Traditional RAS	**SVP RAS**
Logic Processors	7	0
I/O Modules	66	0
SVPs	0	6
Ethernet Switches	0	6
Wiring	730 wires/cables	30 cables
Power	470 W	210 W
Operate Time	5 Cycles	4.25 Cycles
Equipment Price	$144,000	$102,000
Installation and Check-out Price	$21,000	$8,000
TOTAL	$165,000	$110,000

VI. Real-Time Voltage Stability

Reference [10] contains a synchrophasor-based real-time voltage stability index (VSI).

Equations (2), (3), and (4) directly calculate the theoretical maximum transferable power (P, Q, and S) from the source to the load of a radial network.

$$P_{max} = \frac{QR}{X} - \frac{V_s^{\,2}R}{2X^2} + \frac{|Z_L|V_s\sqrt{V_s^{\,2} - 4QX}}{2X^2} \tag{2}$$

$$Q_{max} = \frac{PX}{R} - \frac{V_s^{\,2}X}{2R^2} + \frac{|Z_L|V_s\sqrt{V_s^{\,2} - 4PR}}{2R^2} \tag{3}$$

$$S_{max} = \frac{V_s^{\,2}\left[|Z_L| - (\sin(\theta)X + \cos(\theta)R)\right]}{2(\cos(\theta)X - \sin(\theta)R)^2} \tag{4}$$

With the calculated P_{max}, Q_{max}, and S_{max}, three load margins (P_{margin}, Q_{margin}, and S_{margin}) can be readily calculated with (5)–(7), respectively. The VSI is derived by taking the minimum of the ratios of the margins to maximum powers (8).

$$P_{margin} = P_{max} - P \tag{5}$$

$$Q_{margin} = Q_{max} - Q \tag{6}$$

$$S_{margin} = S_{max} - S \tag{7}$$

$$VSI = \min\left(\frac{P_{margin}}{P_{max}}, \frac{Q_{margin}}{Q_{max}}, \frac{S_{margin}}{S_{max}}\right) \tag{8}$$

For meshed transmission networks, researchers have developed several methods, like the REI network equivalent method [11], to quickly approximate the electrical distance from generation sources to individual loads by knowing the status of the power system and, therefore, allowing estimation of the maximum loading condition for the corresponding load bus.

Synchrophasor technology provides the status of the power system at a much faster rate than traditional power system state estimators or other similar measurement systems such as SCADA. The SVP can receive, process, and notify operators of voltage instability conditions within local areas as well as large areas. Further, the result of voltage stability assessment calculations can be directly incorporated into remedial action schemes to improve power system security.

VII. Power System State Determination

To provide reliable power, utilities perform power system security analysis. The state of the power system must be determined. Schweppe [12], [13], [14] introduced state estimation, which has developed into a highly-refined science. Reference [15] is a relatively recent book on state estimation.

The condition of the power system can be determined if the model of the network and the phasor voltages at all buses are known. To see this, consider the matrix equation:

$I = Y V$,

where:

I is a vector of the branch current phasors

V is the vector of bus voltage phasors and

Y is the bus admittance matrix.

If we know Y and V, then we can calculate the currents. Once we know the currents, we can calculate watts, vars, losses, etc.

Unfortunately, SCADA does not provide voltage PHASORS (just voltage MAGNITUDES); there are measurement errors; there are inaccuracies in the system parameters that go into Y; and communications errors can lead to missing analog measurements and to errors in constructing Y. To further add to the challenge of estimating the state, the SCADA measurements available are not taken simultaneously. Instead, they are taken over a period of a few seconds, leading to the possibility that the data really come from more than one system. For example, if half the measurements are received and then a breaker operates, we have a new system, and the next half of the measurements are from a different physical system.

SCADA measurements of voltage magnitudes, watt and var flows on lines, load measurements, generator outputs, the status of breakers and switches, the position of tap changers, and the physical parameters of lines, transformers, and capacitor banks are the inputs to the state-estimation process. Current magnitudes are used to some degree but cannot be relied upon because there can be two power-flow solutions, only one of which corresponds to reality.

The state estimator then performs the following functions:

- *Topology Processor*. Gathers status data about the circuit breakers and switches, and configures the one-line diagrams of the system.
- *Observability Analysis*. Determines if a state estimation solution for the entire system can be obtained using available data.
- *State Estimation Solution.* Determines the optimal estimate of the complex voltages at all the buses. Weighted least squares methods are typical.
- *Bad Data Processing*. Detects the existence of gross errors in the measurement set.
- *Parameter and Structural Error Processing.* Estimates various network parameters, such as transmission line model parameters, tap changing transformer parameters, and shunt capacitor or reactor parameters. Detects structural errors in the network configuration and identifies the erroneous breaker status, provided there is enough measurement redundancy.

When the system is in steady state, the measured quantities are constant with the gathering window; thus, the time skew between measurements does not introduce errors. The location of each measurement is chosen so that there are enough data to estimate the voltage magnitudes and angles at all buses with respect to an angle reference [16].

Traditional state estimators can fail to converge if, for example, the system state is changing faster than the SCADA scan rate or when critical data are missing because of communications channel failures, etc. When the power system state is changing quickly, measurements taken in a single SCADA scan are inconsistent. The inconsistencies between any two analog measurements are proportional to the time difference between the measurements and the rate at which the states are

changing. Additionally, rapid changes in system states are often caused by changes in the topology of the system like a fault, transformer tap change, switch operation, etc. When topology changes are undetected or happen during the SCADA data polling, the estimation is likely to fail because state estimation is quite dependent on the bus-admittance matrix.

Let's revisit our matrix equation I = Y V and the objective of determining the system state, with synchronous phasor measurements in mind:

1. Synchronous phasor measurements are taken at precisely controlled instants of time, eliminating the time-skew source of errors mentioned earlier.
2. We measure the magnitude *and* the angle of voltage, so the angle need not be estimated.
3. We measure the magnitude *and* the angle of current.
4. We measure contact status to the millisecond or better, greatly reducing errors in building the bus admittance matrix.
5. Because we are directly measuring the voltage and current phasors, we can directly compute watt and var flows at the substation or at the master, and associate those calculations with a precise moment in time.
6. There is some redundancy in measurements at the substation. We can use this redundancy to refine locally-derived measurements, such as average voltages, and to find measurement errors locally, and avoid sending them up the chain of command.

Because PMCU measurements are synchrophasors with respect to a global angle reference, the number of critical measurements is less than the state estimator using traditional SCADA measurements. Having direct angle measurements from the PMCUs diminishes the amount of error introduced by inaccuracies in network parameters. For example, consider the three-bus power system shown in Fig. 13. If PMCU data are available from each bus, the state is known immediately. It is the complex voltage at each of the three buses, i.e., three magnitudes and three angles. If, on the other hand, traditional SCADA data are available from the same three buses, only the three voltage magnitudes are measured directly. The three voltage angles have to be calculated using voltage magnitudes, real power measurements, reactive power measurements, line parameters, breaker states, and an angle reference. Fig. 13 shows SCADA measurements used to calculate the voltage angles; however, the quality of the results depends largely on the quality of the network parameters, which are not always accurate. PMCU measurements provide more direct and more accurate information than traditional SCADA measurements because PMCU measurements do not depend on network parameters.

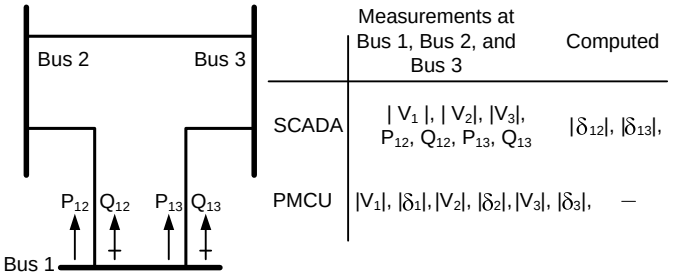

Fig. 13. SCADA and SVP Direct State Measurement

Reference [17] suggests the use of a SuperCalibrator that: (a) performs state estimation on each subsystem using all available data from SCADA, relays, PMUs, meters, etc. and a three-phase breaker-oriented, instrumentation inclusive model, (b) performs bad data identification and rejection as well as topology error identification on each subsystem, (c) performs alarm processing on each subsystem to identify root cause events, and (d) resolves problems for the overlapping parts of the subsystems (state estimation coordination).

The SVP at the substation level can estimate the best voltage, current, and angle measurements of that substation because of the redundant measurement nature of the PMCUs that are monitoring various points within a substation. These estimations can then be forwarded to the state estimator.

Synchrophasor measurements make irrelevant the need for watt and var measurements to determine phase information. Synchrophasor current and voltage measurements, with precision timestamps, directly relate to the phase of the power system with respect to voltage and current measurements. Further, the voltage, currents, and respective phase angles can be used to derive real, imaginary, and apparent power. The SVP collects the various voltage and current measurements and derives phase relations as linear calculations instead of solutions to nonlinear equations that may have multiple solutions.

A traditional state estimator relies on receiving correct data in a timely manner from a single source at each location within a power system. Recall that if incorrect or missing data occur within a calculation period, the state estimator will not converge. An SVP system can be configured to minimize these limitations. Consider the simple three-bus network in Fig. 14. We place an SVP at each bus. The first function of the SVPs is to collect voltage, current, associated phase angles, and bus topologies required for the state estimator. Further, each SVP is configured to exchange synchrophasor information with adjacent SVPs. This redundancy provides backup communications paths to the state estimator in the event that the primary communications link becomes disabled.

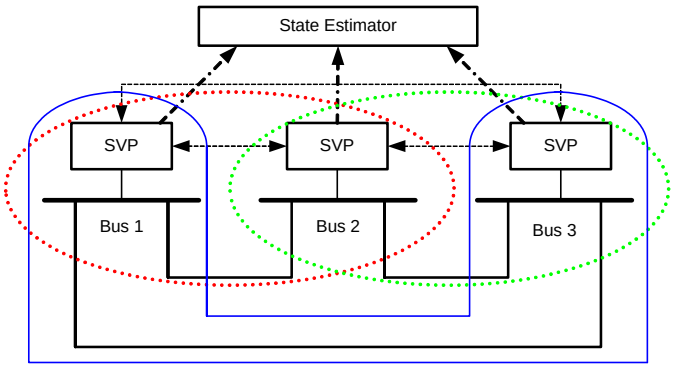

Fig. 14. SVP Peer-to-Peer Communication

This configuration has multiple benefits. Should the communications channel between an SVP and the state estimator fail, an adjacent SVP could forward the data, keeping the state estimator running.

Another approach is to collect and validate local-area data before sending the data to the state estimator. In effect, the SVPs perform local-area state estimation and forward the results to a wide-area state estimator. Fig. 15 shows a representation of the local-area SVPs relative to the state estimator.

Validation and processing steps easily performed by local or regional SVPs include the following:

1. Averaging and qualifying multiple voltage measurements at one substation. Summing feeder or line currents vectorially and comparing them to the transformer-bushing current measurements.
2. Detecting and resolving discrepancies between breaker states and current measurements.
3. Estimating the voltage at adjacent substations using the line parameters and local measurements of current and voltage.
4. Comparing adjacent substation estimates of local voltage against direct measurement of local voltage.

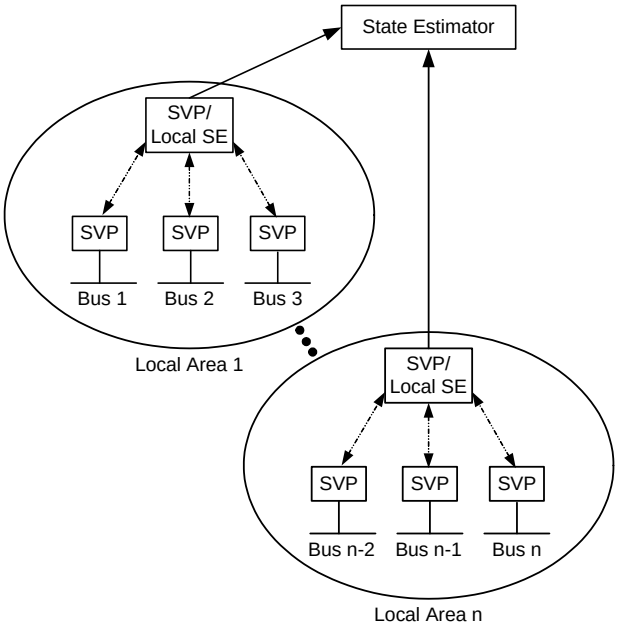

Fig. 15. SVP Local-Area State Estimation

Using a distributed, subarea state estimation approach can detect topology errors sooner in the estimation process, shortening the actual state estimation process.

The SVP provides local logic to make intelligent topology estimations. For example, if a switch status is indicating "open" but current is measured flowing through the associated branch, then the topology information is in error. For this case the SVP would modify the digital topology data to indicate that the switch is closed. This local activity directly reduces the work required to estimate the entire wide-area state, and also reduces the risks of nonconvergence.

VIII. Other Applications

- *Automatic Synchronizing System for One or More Generators.* Bring synchronous phasor measurements together from one or more machines and buses into an SVP. Program the SVP to check and control synchronism in a coordinated way. Calculate watt and var flows, control governors, and exciters to balance the plant.
- *Control and Monitoring of Phase-Shifting Transformers.* Directly measure the phase shift on each phase and compare to the set point.
- *Backup Bus Protection.* Add currents vectorially to create backup bus zones.
- *Voltage-Stability Assessment System.* Measure angles between transmission bus and distribution buses to observe stability margins. Alarm or shed load if needed.
- *Determine the Voltage Phasors at Remote Buses.* Consider a distribution bus, with multiple feeders and voltage regulators. Estimate the voltages at remote buses, possibly at key customers, by compensating the bus voltage with the regulator settings and impedances, and then by calculating the voltage drops along the feeders.
- *Power System Service Recorders.* Bring synchrophasor measurements of currents and voltages into an SVP once per second, format them, and send them to a mass storage device. This provides a permanent record of service at each station and substation.
- *Synchrophasor Negative-Sequence Current Differential Element*. Use the synchrophasor-based negative-sequence differential element for transmission line backup protection. This element provides very high fault resistance coverage with balanced and unbalanced prefault conditions. This element has successfully detected faults with more than 800 ohms of fault resistance [18].
- *Power Swing Detection*. Implement a power swing detection algorithm using the angle difference between two power system areas to calculate slip frequency and acceleration to detect unstable operating conditions. The SVP calculates the angle difference and acceleration using positive-sequence voltage synchrophasors [18].

IX. Conclusions

Now that synchronous phasor measurements are broadly available from protective relays and meters, it is time to put them to work to improve our power systems. The Synchrophasor Vector Processor makes real-time applications practical. Synchrophasor measurements are available at high speeds via C37.118, and medium speeds (still real time) via IEC 61850, DNP3, and Fast Meter protocols. The SVP can perform calculations on these data for refining measurements for SCADA and the existing state estimator, detecting instrument transformer problems, anticipating voltage collapse, measuring critical angles, and virtually any application involving vector mathematics. The SVP can close the loop, effecting control via the programmable outputs in the relays and meters or using independent control devices.

Direct state measurement is now practical because of the widespread availability of synchronous phasor measurements. The SVP plays a role in direct state measurement and can actually reduce the amount of information communicated to the master station. The SVP can average the voltage readings from a number of sensors, preparing one optimal measurement to send to the master. Using simple linear calculations at nearby stations or at the master, the SVP can also estimate voltage phasors at buses that do not have local synchronous phasor measurements. With synchronous measurements, we can actually communicate *less* information to the master to have the same level of knowledge of the state of the power system.

Finally, we have shown that practical and economically important solutions can be built today, frequently using relays and meters already installed.

X. Acknowledgment

The authors wish to thank Armando Guzmán, Marcos Donolo, and Yanfeng Gong for their contributions.

XI. Appendix A. Synchronous Phasor Measurement Communications Methods and Their Performance

- *IEEE C37.118.* This open standard describes how to measure and format synchronized phasor measurements in power systems. It addresses the definition of a synchronized phasor, microsecond time synchronization, application of timetags, method to verify measurement compliance with the standard, and message formats generated by PMCUs to PDCs. C37.118 does not specify a preferred physical layer e.g., Ethernet or serial. Presently C37.118 specifies data rates up to thirty messages per second. These messages are continually sent from the PMCU. C37.118 does not specify a method for issuing control commands to a PMCU, i.e., a specific message format sent from a PDC/SVP to a PMCU. However, there are user-defined bits within a configuration field that may be used, e.g., a trip command may be sent in a PDC to PMCU command message. This is a vendor-specific solution.
- *Fast Message (FM).* This proprietary standard is capable of both sending and receiving data in a master-slave network configuration. FM may operate over serial or Ethernet communications links. The FM protocol does NOT include timestamp information. Typical analog data from a PMCU using FM are on the order of 300 milliseconds. Typical control commands received by a PMCU using FM are executed within eight milliseconds.
- *IEC 61850.* This open standard consists of various protocols. IEC 61850 GOOSE allows for both analog and digital peer-to-peer data exchange. The communications link is Ethernet based. The standard does include timetags associated with messages. The timetag accuracy is on the order of milliseconds. Messages may be exchanged asynchronously and testing has shown that processing of digital data is on the order of eight to twelve milliseconds.
- *DNP3.* This open standard is capable of both sending and receiving data in a master-slave network configuration (except intermaster station communications). DNP3 may operate over serial or Ethernet communications links. The standard does include timetags associated with messages. The timetag accuracy is on the order of milliseconds. Messages may be exchanged asynchronously (a function of the polling/response rate). Processing throughput rates are vendor-dependent but can be as fast as twenty milliseconds.
- *Modbus.* This open standard is capable of both sending and receiving data in a master-slave network configuration. Modbus may operate over serial or Ethernet communications links. The standard does NOT include timetags associated with messages. The timetag accuracy is on the order of milliseconds. Messages may be exchanged asynchronously (a function of the polling/response rate). Processing throughput rates is vendor-dependent but can be in the eight millisecond range.

Table II summarizes SVP communications protocols performance parameters.

TABLE II
SVP Protocol Performance Parameters

	Communications	**Send Data**	**Receive Data**	**Processing Throughput (typical)**	**Timestamp Accuracy**
C37.118	Ethernet or Serial	Yes	No*	1 cycle	microseconds
FM Synchrophasor	Ethernet or Serial	Yes	No	50 milliseconds	microseconds
FM	Ethernet or Serial	Yes	Yes	300 milliseconds	Not available
IEC 61850	Ethernet	Yes	Yes	12 milliseconds	milliseconds
DNP	Ethernet or Serial	Yes	Yes	20 milliseconds	milliseconds
Modbus	Ethernet or Serial	Yes	Yes	8 milliseconds	Not available

* Not specifically defined by standard, however, methods can be devised to use control fields in a nonstandard fashion to achieve limited data reception.

XII. Appendix B. Communications and Control Capabilities of Synchrophasor Devices

Presently there are various types of PMUs available, those that monitor and others that monitor and control.

Monitoring PMUs consist of stand-alone PMUs, digital fault recorders with synchrophasor capabilities, and similar devices. Monitoring PMUs generally lack the capability to trip/close a breaker.

Control PMUs, or PMCUs, consist of relays, meters, and other similar devices. Control PMUs have these advantages over monitoring PMUs:

- Wide distribution throughout a power system.
- Monitor voltages, currents, breaker status, switch status, etc. There is no need for more equipment.
- Digital I/O designed to interface with primary equipment in substations.
- Substation hardened, i.e., designed and tested to C37 and IEC electrical and environmental standards.

Using a control PMCU with an SVP provides a reliable, cost effective way to use synchrophasors in wide-area control schemes.

XIII. References

[1] "IEEE Standard for Synchrophasors for Power Systems," IEEE Std C37.118-2005. See http://standards.ieee.org/.

[2] K. E. Martin, "Synchronized System Measurement Networks in North America: Operating Process and System Formats Based Upon BPA's Phasor Data Concentrator," WAMS Working Note, June 1, 2004. Available at ftp://ftp.bpa.gov/pub/WAMS_Information/PDC_System%26 Formats040601.doc.

[3] SEL-3306 Synchrophasor Processor, available at http://www.selinc.com/ sel-3306.htm.

[4] G. J. Cokknides, A. P. S. Meliopoulos, G. Stefopoulous, R. Alaileh, A. Mohan, "Visualization and Characterization of Stability Swings via GPS-Synchronized Data," *Proceedings of the 40th Annual Hawaii International Conference on System Sciences*, Waikoloa, Big Island, Hawaii, January 2007.

[5] C. Gillis, "NOAA 2007-R206, Researchers Find Global Positioning System Is Significantly Impacted by Powerful Solar Radio Burst," news release available at http://www.publicaffairs.noaa.gov/ releases2007/apr07/noaa07-r206.html.

[6] K. Behrendt, K. Fodero, "The Perfect Time: An Examination of Time-Synchronization Techniques," *Proceedings of the 33rd Annual Western Protective Relay Conference*, Spokane, WA, October 2006.

[7] G. Benmouyal, E. O. Schweitzer, A. Guzmán, "Synchronized Phasor Measurement in Protective Relays for Protection, Control, and Analysis of Electric Power Systems," *Proceedings of the 29th Annual Western Protective Relay Conference*, Spokane, WA, October 2002.

[8] "IEC 61131-3 Programmable Controllers—Part 3: Programming Languages," January 21, 2003, available at http://webstore.iec.ch/webstore /webstore.nsf/artnum/029664.

[9] "IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems," IEEE Std 1588-2002. See http://standards.ieee.org/.

[10] Y. Gong, N. Schulz, A. Guzmán, "Synchrophasor-Based Real-Time Voltage Stability Index," *Proceedings of the 32nd Annual Western Protective Relay Conference*, Spokane, WA, October 2005.

[11] F. F. Wu, N. Narasimhamurti, "Necessary Conditions for REI Reduction to be Exact," *IEEE PES Winter Meeting 1979*, Paper A 79 065-4, 1979.

[12] F. C. Schweppe, J. Wildes, "Power System Static-State Estimation, Part I: Exact Model," *IEEE Transactions on Power Apparatus and Systems*, Vol. PAS-89, January 1970, pp. 120–125.

[13] F. C. Schweppe, D. B. Ron, "Power System Static-State Estimation, Part II: Approximate Model," *IEEE Transactions on Power Apparatus and Systems*, Vol. PAS-89, January 1970, pp. 130–135.

[14] F. C. Schweppe, "Power System Static-State Estimation, Part III: Implementation," *IEEE Transactions on Power Apparatus and Systems*, Vol. PAS-89, January 1970, pp. 130–135.

[15] A. Abur, A. G. Exposito, *Power System State Estimation, Theory and Implementation*, New York: Marcel Dekker, 2004.

[16] M. Donolo, "Advantages of Synchrophasor Measurements," Application Note AN2006-10, Schweitzer Engineering Laboratories, Inc., 2006. Available at http://www.selinc.com/appnotes.htm.

[17] A. P. S. Meliopoulos, G. J. Cokkinides, F. Galvan, B. Fardanesh, P. Myrda, "Advances in the SuperCalibrator Concept–Practical Implementations," *Proceedings of the 40th Annual Hawaii International Conference on System Sciences*, Waikoloa, Big Island, Hawaii, January 2007.

[18] A. Guzmán, V. Mynam, G. Zweigle, "Backup Transmission Line Protection for Ground Faults and Power Swing Detection Using Synchrophasors," *Proceedings of the 34th Annual Western Protective Relay Conference*, Spokane, WA, October 2007.

XIV. Biographies

Dr. Edmund O. Schweitzer, III is recognized as a pioneer in digital protection and holds the grade of Fellow of the IEEE, a title bestowed on less than one percent of IEEE members. In 2002 he was elected a member of the National Academy of Engineering. He is the recipient of the Graduate Alumni Achievement Award from Washington State University and the Purdue University Outstanding Electrical and Computer Engineer Award. In September 2005, he was awarded an honorary doctorate from Universidad Autónoma de Nuevo León in Monterrey, Mexico, for his contribution to the development of electric power systems worldwide. He has written dozens of technical papers in the areas of digital relay design and reliability and holds more than 30 patents pertaining to electric power system protection, metering, monitoring, and control. Dr. Schweitzer received his Bachelor's degree and his Master's in electrical engineering from Purdue University, and his PhD degree from Washington State University. He served on the electrical engineering faculties of Ohio University and Washington State University, and in 1982 he founded Schweitzer Engineering Laboratories, Inc. to develop and manufacture digital protective relays and related products and services. Today SEL is an employee-owned company, which serves the electric power industry worldwide, and is certified to the international quality standard ISO-9001. SEL equipment is in service at voltages from 5 kV through 500 kV, to protect feeders, motors, transformers, capacitor banks, transmission lines, and other power apparatus.

David Whitehead, P.E. is the vice president of Research and Development at Schweitzer Engineering Laboratories, Inc. Prior to joining SEL, he worked for General Dynamics, Electric Boat Division as a combat systems engineer. He received his BSEE from Washington State University in 1989, his MSEE from Rensselaer Polytechnic Institute in 1994, and is pursuing his PhD at the University of Idaho. He is a registered professional engineer in Washington State and Senior Member of the IEEE. Mr. Whitehead holds seven patents with several others pending. He has worked at SEL since 1994 and has been responsible for the design of advanced hardware, embedded firmware, and PC software as hardware engineer, research engineer, and chief engineer/assistant director.

Previously presented at the 2008 Texas A&M Conference for Protective Relay Engineers.

20070911 • TP6295-01