Reactive Power Control System for Wind Farm Application Using IEC 61850

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***Abstract*—Wind generating facilities often require significant reactive power (VAR) support to maintain voltage and power factor within the operating limits prescribed by the transmission grid entity that supplies the tie to the grid. VAR support is often provided by multiple stages of capacitor banks connected to the wind farm collector buses that can be switched in and out. Commercially available capacitor bank controllers are not capable of controlling multiple capacitor banks in a coordinated and unified manner.**

This paper discusses an integrated protection and control system that utilizes a central capacitor controller to regulate both power factor and voltage at the point of utility interconnection. The challenge when using multiple regulation parameters is to prevent hunting due to conflicts between the control requirements. An adaptive algorithm was developed to deal with this challenge. The control communicates with up to eight capacitor group relays using IEC 61850 GOOSE (Generic Object-Oriented Substation Event) messaging over an Ethernet network. Each capacitor group relay provides overcurrent protection for the overall capacitor group and neutral voltage unbalance protection for the individual capacitor banks in the group. The capabilities of IEC 61850 as an enabling technology greatly simplified the design and implementation of this complex system of multiple devices.

I. Introduction

Wind generating facilities often require significant reactive power (VAR) support to maintain voltage and power factor within the operating limits prescribed by the transmission grid entity that supplies the tie to the grid. VAR support is often provided by multiple stages of capacitor banks connected to the wind farm collector buses that can be switched in and out. The capacitor banks are configured with multiple capacitor group main circuit breakers with four to six individual capacitor banks switched by vacuum switches in each group.

Commercially available capacitor bank controllers are not capable of controlling multiple capacitor banks in a coordinated and unified manner. The capacitor bank controller typically cannot provide protection for the capacitor banks.

This paper discusses an integrated protection and control system that utilizes a central capacitor controller to regulate both power factor and voltage at the point of utility interconnection. The controller works in concert with capacitor group relays on each capacitor group main circuit breaker. Each capacitor group relay provides overcurrent protection for the overall capacitor group and neutral voltage unbalance protection for the individual capacitor banks in the group, as well as auto/manual control features and a sequencing algorithm to even out the switching operations for the capacitor bank switches.

The challenge when using multiple regulation parameters is to prevent hunting due to conflicts between the control requirements. An adaptive algorithm was developed to deal with this challenge. The regulation algorithms were verified and fine-tuned using a Real Time Digital Simulator (RTDS®).

The engineers applying the system wanted it to be easily configurable so that it could be deployed in support of many varied wind farm projects. They did not want to have to return to the custom control system designers to have the system configured to cover variations in each project. To make it appear that the programmable relays are dedicated capacitor protection and control devices, a custom graphical user interface (GUI) was developed that works inside the original equipment manufacturer (OEM) settings software environment. A complete instruction manual for the system was also developed.

II. Overview of the Protection and Control System

Fig. 1 shows a simplified one-line diagram of the protection and control system. The control (Device 90) measures power flow at the point that ties the facility to the utility system. It measures three-phase voltage, real and imaginary power flow, and power factor (ratio of real power, P, to apparent power, S) towards the utility system. It also monitors single-phase voltage on up to three independent collector buses. The controller uses collector bus voltage magnitude to determine the dead/live status of the collector bus and to determine the expected change in reactive power (ΔQ) per step for capacitor banks connected to that collector bus.

A. Control, Device 90

The control sends commands via IEC 61850 GOOSE (Generic Object-Oriented Substation Event) messages over an Ethernet channel to each capacitor group relay (Device 51/59N). The commands are sent according to a first in, first out (FIFO) sequencing algorithm, which adds or removes capacitor banks in order to maintain the power factor between leading and lagging limits, as well as the voltage between upper and lower limits. If the power factor and voltage limits do not conflict, either out-of-band condition results in the addition or removal of a capacitor bank.

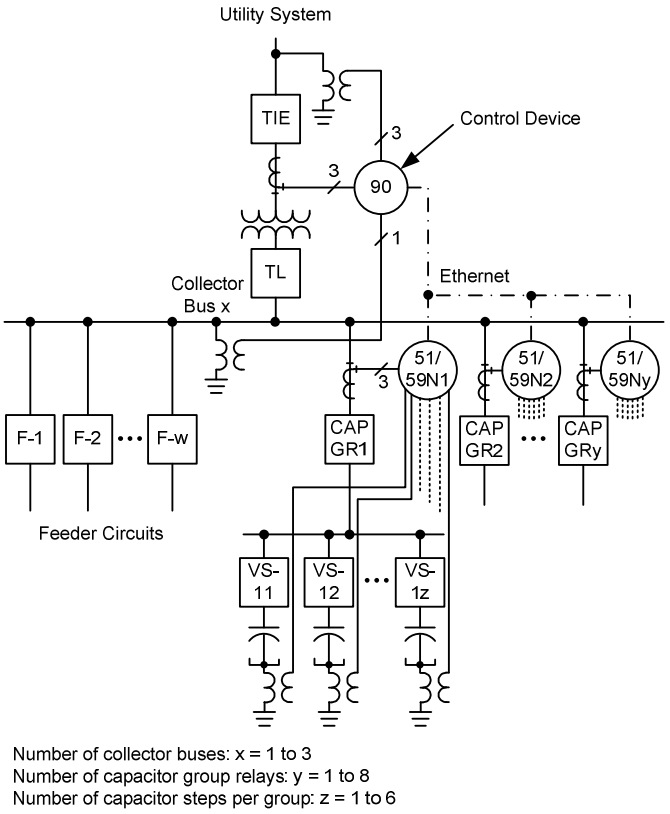

Fig. 1. Simplified one-line diagram

A user-settable option determines which measure has priority if the power factor and voltage criteria are in conflict. For example, if the facility is consuming too many VARs supplied by the utility, resulting in the power factor being out-of-band leading, the control will want to add capacitors. But, if the voltage is out-of-band high, the control will want to remove capacitors. Under this condition, if the user selects power factor priority, the control will add capacitors to correct the power factor. If the user selects voltage priority, the control will remove capacitors to correct the voltage.

Alarms indicate if the regulated parameters are outside of band limits. These alarms will assert if, for example, the power factor is out of band but cannot be corrected, because the voltage is out of band and voltage priority has been selected. Or they will assert if the regulated parameters are out of band but the control cannot add or remove capacitor banks, because the group relays indicate that there are no capacitor banks available to switch.

The control also includes dead-bus sensing on up to three collector buses. When a dead bus is detected, the control device sends the status to every capacitor group relay on that bus. The capacitor group relay then trips the main breaker of the capacitor group and opens all of its vacuum switches and places them in manual mode. When the live bus is asserted, the dead bus status is deasserted.

B. Capacitor Group Relays, Device 51/59N

The capacitor group relays communicate with the control device to indicate whether there is a capacitor bank within its group that is available to add or remove. This information is used in the control's sequencing algorithm. If the capacitor group relay receives a command to add or remove a capacitor bank, the capacitor bank vacuum switches are opened and closed in turn according to the capacitor group relay's own FIFO sequencing algorithm for its group. A capacitor bank vacuum switch must be in automatic mode before it can be available for automatic addition or removal. The relay also prevents a capacitor bank from being available to add for a user-settable dead time after it has been removed in order to allow the capacitors to discharge.

In addition to controlling the automatic switching of the capacitor banks, the capacitor group relays provide protection. Phase and ground as well as time and instantaneous overcurrent (50P, 51P, 50N, and 51N) elements are available for the main breaker of the capacitor group. Alarm and trip levels for neutral overvoltage (59N1, 59N2, 59N3, 59N4, 59N5, and 59N6) elements are available for up to six capacitor banks in each capacitor group.

The relay includes breaker failure (50BF) protection for the capacitor group main circuit breaker and the capacitor bank vacuum switches.

III. IEC 61850 GOOSE Message Signaling

Table I shows the status signals that the control device receives via IEC 61850 GOOSE messaging. It receives three status bits from up to eight capacitor group relays. A fourth status bit for each capacitor group relay allows the control device to monitor the status of communications with the relays. These devices identify incoming discrete message contents as communications card inputs (CCINs) and outgoing discrete message contents as communications card outputs (CCOUTs).

TABLE I
ASSOCIATION OF INCOMING GOOSE MESSAGE CONTENTS TO INTERNAL CONTROL DEVICE LOGIC ELEMENTS (CCINS)
(CCIN041 – CCIN128 NOT SHOWN)

Input	Purpose	Input	Purpose
CCIN001	Group 1, capacitor available to add	CCIN021	Group 1, add/remove in process
CCIN002	Group 2, capacitor available to add	CCIN022	Group 2, add/remove in process
CCIN003	Group 3, capacitor available to add	CCIN023	Group 3, add/remove in process
CCIN004	Group 4, capacitor available to add	CCIN024	Group 4, add/remove in process
CCIN005	Group 5, capacitor available to add	CCIN025	Group 5, add/remove in process
CCIN006	Group 6, capacitor available to add	CCIN026	Group 6, add/remove in process
CCIN007	Group 7, capacitor available to add	CCIN027	Group 7, add/remove in process
CCIN008	Group 8, capacitor available to add	CCIN028	Group 8, add/remove in process
CCIN009		CCIN029	
CCIN010		CCIN030	
CCIN011	Group 1, capacitor available to remove	CCIN031	Group 1, communications alarm
CCIN012	Group 2, capacitor available to remove	CCIN032	Group 2, communications alarm
CCIN013	Group 3, capacitor available to remove	CCIN033	Group 3, communications alarm
CCIN014	Group 4, capacitor available to remove	CCIN034	Group 4, communications alarm
CCIN015	Group 5, capacitor available to remove	CCIN035	Group 5, communications alarm
CCIN016	Group 6, capacitor available to remove	CCIN036	Group 6, communications alarm
CCIN017	Group 7, capacitor available to remove	CCIN037	Group 7, communications alarm
CCIN018	Group 8, capacitor available to remove	CCIN038	Group 8, communications alarm
CCIN019		CCIN039	
CCIN020		CCIN040	

The implementation of IEC 61850 GOOSE messaging in the devices includes a message quality function that asserts when a message is corrupted, does not match the expected configuration, or is not received when expected. The protocol allows the user to set the cyclic refresh rate to a short interval, which results in nearly continuous monitoring of the channel. This Message Quality bit from the Ethernet processor card is mapped to a CCIN bit in the control device and each relay to alarm for a communications link failure. Here, it is used to create the "Group *n*, communications alarm" or the "control communications alarm."

Table II shows the command message signals that the control device sends via IEC 61850 GOOSE messaging. Using a single message, it sends three unique command bits to as many as eight capacitor group relays.

TABLE II
ASSOCIATION OF INTERNAL CONTROL DEVICE LOGIC ELEMENTS TO OUTGOING GOOSE MESSAGE CONTENTS (CCOUTS)

Output	Purpose	Output	Purpose
CCOUT001	Add capacitor step, Group 1	CCOUT017	Remove capacitor step, Group 7
CCOUT002	Add capacitor step, Group 2	CCOUT018	Remove capacitor step, Group 8
CCOUT003	Add capacitor step, Group 3	CCOUT019	
CCOUT004	Add capacitor step, Group 4	CCOUT020	
CCOUT005	Add capacitor step, Group 5	CCOUT021	Open main, dead bus, Group 1
CCOUT006	Add capacitor step, Group 6	CCOUT022	Open main, dead bus, Group 2
CCOUT007	Add capacitor step, Group 7	CCOUT023	Open main, dead bus, Group 3
CCOUT008	Add capacitor step, Group 8	CCOUT024	Open main, dead bus, Group 4
CCOUT009		CCOUT025	Open main, dead bus, Group 5
CCOUT010		CCOUT026	Open main, dead bus, Group 6
CCOUT011	Remove capacitor step, Group 1	CCOUT027	Open main, dead bus, Group 7
CCOUT012	Remove capacitor step, Group 2	CCOUT028	Open main, dead bus, Group 8
CCOUT013	Remove capacitor step, Group 3	CCOUT029	
CCOUT014	Remove capacitor step, Group 4	CCOUT030	
CCOUT015	Remove capacitor step, Group 5	CCOUT031	
CCOUT016	Remove capacitor step, Group 6	CCOUT032	

Table III shows commands that the relays receive via IEC 61850 GOOSE messaging. They receive three command bits from the control. A fourth status bit for each capacitor group relay allows the communications card to indicate the status of communications with that device.

TABLE III
ASSOCIATION OF INCOMING GOOSE MESSAGE CONTENTS TO INTERNAL RELAY LOGIC ELEMENTS (CCINS)
(CCIN011 – CCIN128 NOT SHOWN)

Input	Purpose	Input	Purpose
CCIN001	Add capacitor bank	CCIN005	
CCIN002	Remove capacitor bank	CCIN006	
CCIN003	Open group circuit breaker for dead bus	CCIN007	
CCIN004	Control communications alarm	CCIN008	
CCIN005		CCIN009	
CCIN006		CCIN010	

Table IV shows the status signals that the relays send via IEC 61850 GOOSE messaging. They send three status bits to the control.

TABLE IV
ASSOCIATION OF INTERNAL RELAY LOGIC ELEMENTS TO OUTGOING GOOSE MESSAGE CONTENTS (CCOUTS)

Output	Purpose	Output	Purpose
CCOUT001	Capacitor bank available to add	CCOUT006	
CCOUT002	Capacitor bank available to remove	CCOUT007	
CCOUT003	Auto add/remove in process	CCOUT008	
CCOUT004		CCOUT009	
CCOUT005		CCOUT010	

IV. CUSTOM LOCAL HUMAN-MACHINE INTERFACE (HMI)

The programmable devices used for the control and relay include fully customizable, front-panel HMI features. Fig. 2 shows the user-programmable LED (light-emitting diode) and pushbutton configuration of the control. In addition, the devices have a fully programmable, rotating LCD (liquid crystal display) to show metering and additional status values.

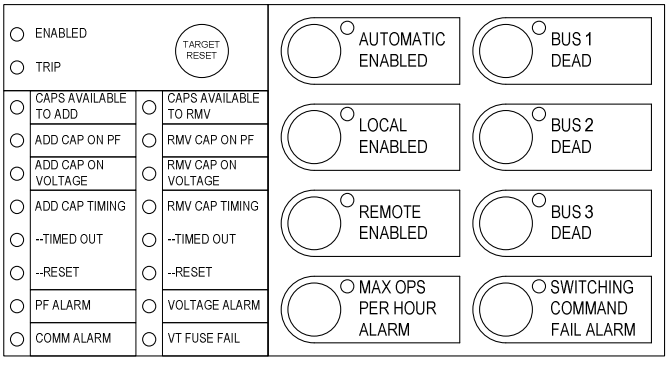

Fig. 2. Capacitor control front panel

The programmable pushbuttons show the status of manual control functions, such as {AUTOMATIC ENABLED}, {LOCAL ENABLED}, and {REMOTE ENABLED}. They also show the status of latched alarms, which can be reset by the operator.

Programmable LEDs show the complete status of the system, including the following:

- Availability of capacitor banks to add or remove.
- Status of power factor and voltage control algorithms.
- Status of timers.
- Conditions of various alarms.

The capacitor group relays have a similarly customized front-panel HMI.

V. OVERVIEW OF CAPACITOR CONTROL FUNCTIONS

A. Control of Reactive Power Supply

The reactive power supply at a facility is important to the reliable and economic operation of the power system. In many cases, utility system operators charge power factor penalties if a facility is consuming too much reactive power. Reactive power support helps control the voltage on the interconnected power grid. Increasing the capacitive VAR supply raises the local bus voltage, while decreasing the capacitive VAR supply lowers the local bus voltage. Voltage support is necessary for power transfer.

The VAR supply can come from dynamic sources, such as rotating machine excitation systems and static compensators (STATCOMs), or from static sources, such as switched capacitor banks. Often, there is a combination of these sources. External sources of reactive power are commonly required for wind generation—the primary application for which this system was developed.

The control monitors bus voltage and power factor and regulates both parameters. As long as the two control parameters are not in conflict, either control function can add or remove capacitors. The user must select between power factor or voltage priority when the two control parameters are in conflict.

B. Regulation Challenges

In the PQ plane, real power (P) and reactive power (Q) are quadrature components. The hypotenuse of the power triangle is the apparent power (S). For this control, one of the regulated quantities is the power factor (PF). PF is the ratio of P/S. However, the controlled quantity is discrete steps of Q. The step size is based upon the size of each switched capacitor bank. PF is a ratio, so at low real power flow, the ΔQ from one step can overshoot the opposite band limit, which would result in hunting. So, the power factor regulation limits must be modified as power flow approaches zero.

Another complicating matter in designing the regulation characteristics is that the expected ΔQ from a switching operation varies by the square of the bus voltage. For this reason, it is desirable to measure the voltage on each collector bus so that the control can adjust its regulation characteristics based upon the actual expected ΔQ, instead of using the nominal VAR rating of the capacitor banks.

For voltage regulation, the change in voltage (ΔV) associated with a step change in local VAR support is a function of the equivalent source impedance to that bus. High source impedance will magnify the capacitive rise associated with a step addition in reactive power. In a wind generation facility, the equivalent source impedance is expected to vary greatly, depending upon how many machines are online.

Other devices, such as wind generator control systems or a load tap changer on the step-up transformer, may also make control responses to regulate the voltage on a bus. The ΔV resulting from a capacitor switching operation may cause a converse reaction in these other voltage control systems. For this reason, it is necessary to consider other control systems at the wind farm facility that may respond to power factor and voltage. Hunting may result if various control systems interact.

VI. Add/Remove Capacitor (Regulation) Logic

A. Power Factor Regulation

Fig. 3 illustrates the power factor control characteristics in the PQ plane. The control has separate leading and lagging power factor limits. The limit in effect depends on the quadrant in which the power system is operating. Since power factor is a ratio of P/S (real power over apparent power) and the controlled quantity is Q, the power factor band limits are cut off when the expected ΔQ will overshoot the opposite power factor band limit. Equations (1) and (2) describe the limits.

$$\mathrm{RCQL} = \frac{\Delta Q_{\mathrm{NextRmv}} \bullet \mathrm{Margin}}{2} \tag{1}$$

$$\mathrm{ACQL} = \frac{\Delta Q_{\mathrm{NextAdd}} \bullet \mathrm{Margin}}{2} \tag{2}$$

where:

RCQL is the remove capacitor VAR limit.

ACQL is the add capacitor VAR limit.

$\Delta Q_{\mathrm{NextRmv}}$ is the ΔQ expected from the next capacitor bank to be removed, per (3).

$\Delta Q_{\mathrm{NextAdd}}$ is the ΔQ expected from the next capacitor bank to be added, per (4).

Margin is the ΔQ margin setting.

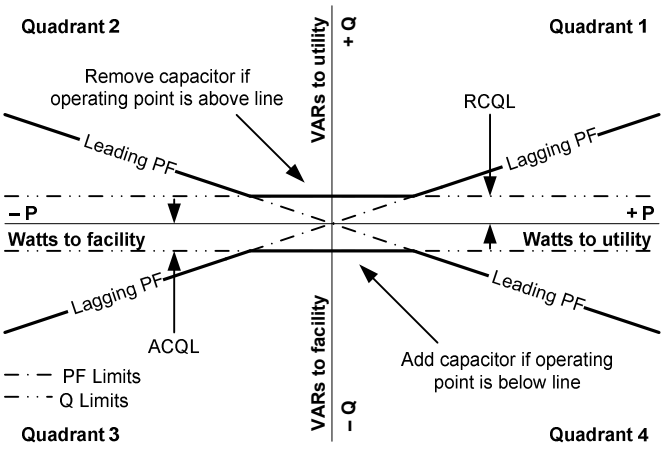

Fig. 3. Power factor regulation characteristic

B. ΔQ Next Capacitor Step Function

The VARs supplied by a capacitor bank vary by the square of the voltage at its terminals. The control adjusts the nominal Q rating (Q_{NOM}) of the capacitor steps, based upon the measured voltage, as shown in (3) and (4). This is the value used to determine the expected ΔQ for the next capacitor to be switched in or out.

$$\Delta Q_{\mathrm{NextRmv}} = \mathrm{VNR}_{\mathrm{PU}}{}^{2} \bullet Q_{\mathrm{NOM}} \tag{3}$$

$$\Delta Q_{\mathrm{NextAdd}} = \mathrm{VNA}_{\mathrm{PU}}{}^{2} \bullet Q_{\mathrm{NOM}} \tag{4}$$

where:

$\Delta Q_{\mathrm{NextRmv}}$ is the change in reactive power expected from the next capacitor bank to be removed.

$\mathrm{VNR}_{\mathrm{PU}}$ is the voltage associated with the next capacitor group to be removed, in per unit.

$\Delta Q_{\mathrm{NextAdd}}$ is the change in reactive power expected from the next capacitor bank to be added.

$\mathrm{VNA}_{\mathrm{PU}}$ is the voltage associated with the next capacitor group to be added, in per unit.

Q_{NOM} is the capacitor step nominal three-phase MVAR rating setting.

The collector bus voltage associated with the next capacitor group to be switched is determined by the capacitor group enable logic. The control measures the voltage on each collector bus and converts it to per unit based upon the capacitor nominal primary voltage rating and the collector bus voltage sensing. Finally, the sequencing logic function determines the next capacitor group to be added or removed and which bus it is on.

C. Voltage Regulation

The voltage high limit and voltage low limit are set in per unit of nominal. If the voltage is out-of-band high, the control will remove capacitors. If the voltage is out-of-band low and above 10 volts secondary, the control will add capacitors. The control uses the positive-sequence voltage for this function.

D. V/Q Priority Logic

If voltage and power factor regulation criteria are in conflict, the control determines which has priority based upon the V/Q priority setting. An example will help to illustrate the need for this function. For this example, the voltage is in band but very near its high limit, and the power factor regulation is out of band and calling for adding a capacitor bank. The ΔQ to correct the power factor will result in the power factor regulation function being satisfied but the voltage regulation function becoming out-of-band high. This will cause the voltage regulation function to remove a capacitor bank to correct the voltage. The situation will continue to toggle, resulting in excessive operations.

The control uses logic, as described in Table V, to prevent conflicts between the two control parameters. See Fig. 4, Fig. 5, Fig. 6, and Fig. 7 for the blocking limit characteristics. The control action of the nonpriority control parameter is blocked when it is within one step of being out of band of the opposite control action (add or remove).

For the Q limit, the regulation limit is offset by the expected ΔQ, as described in Part B of this section. For the V limit, the regulation limit is offset by the average ΔV from the six most recent switching operations.

TABLE V
V/Q PRIORITY LOGIC

Priority Setting	Control Function	Supervision Logic	Figure
PF (Q)	Add capacitor on voltage	But not if Q > Q priority add capacitor Q limit	Fig. 4
PF (Q)	Remove capacitor on voltage	But not if Q < Q priority remove capacitor Q limit	Fig. 5
V	Add capacitor on PF	But not if V > V priority add capacitor V limit	Fig. 6
V	Remove capacitor on PF	But not if V < V priority remove capacitor V limit	Fig. 7

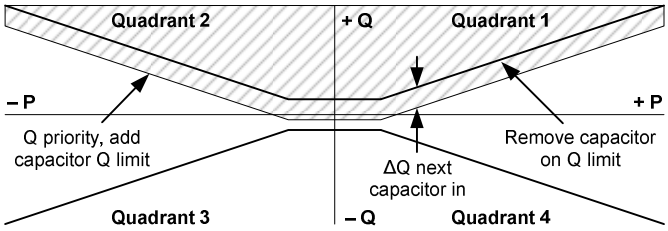

Fig. 4. Q priority, add capacitor on voltage blocking characteristic

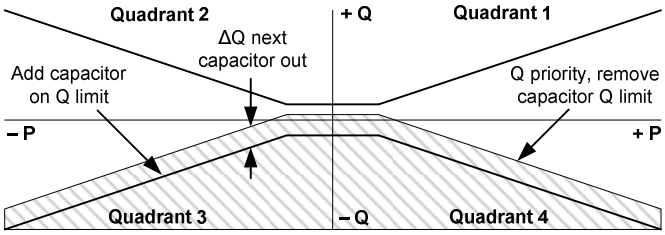

Fig. 5. Q priority, remove capacitor on voltage blocking characteristic

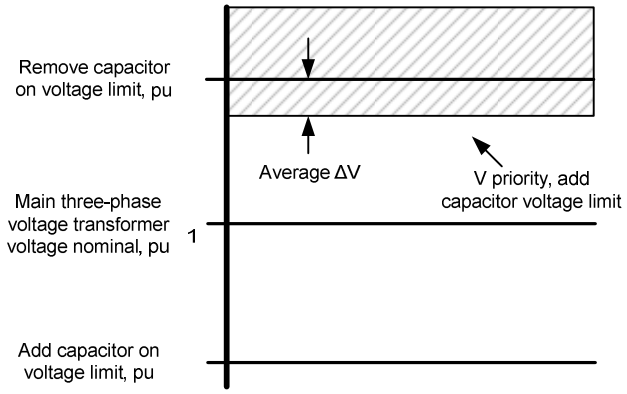

Fig. 6. V priority, add capacitor on power factor blocking characteristic

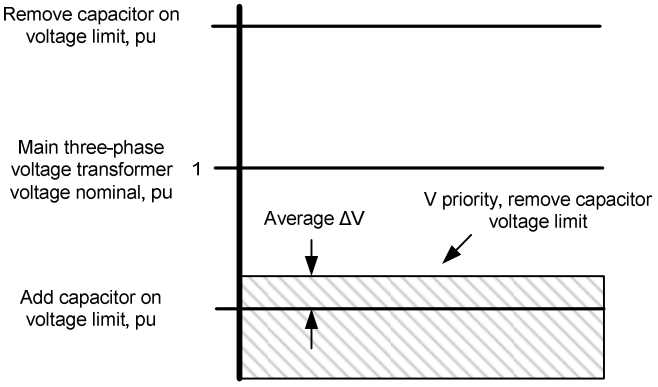

Fig. 7. V priority, remove capacitor on power factor blocking characteristic

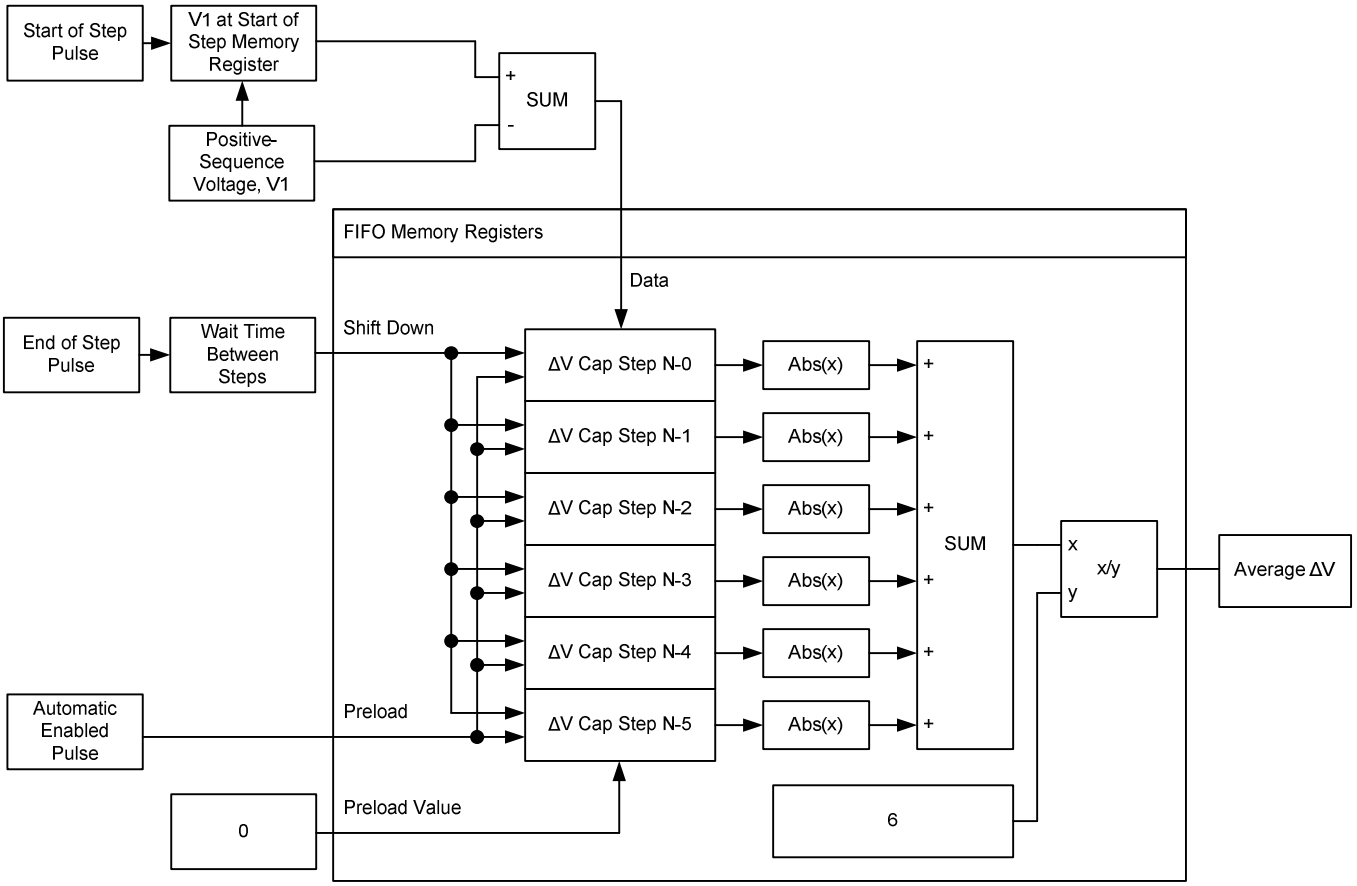

Fig. 8. ΔV FIFO memory and average function

E. Average ΔV Function

Since the ΔV associated with each step is expected to vary based upon system conditions, the control records the ΔV associated with each switching operation in a six-register FIFO memory buffer and averages them for use by the V/Q priority logic. See Fig. 8.

F. Integrating Timers Function

The integrating timers function provides a time delay to ensure that the control parameters are out of band for a specified period of time before a switching operation is initiated. If automatic control is enabled, once one of the controlled parameters goes out-of-band high or out-of-band low for a set time delay, a switching command will be initiated in the correct direction to move the regulated parameter back in band. The integrating timers count up when the parameter (voltage or power factor) is out of band and count down when it is in band.

One way to understand the characteristics of an integrating timer is to envision the hand of a clock that moves clockwise or counterclockwise, depending on which input is asserted, as shown in Fig. 9. When the hand is against the reset stop, the timer is reset. If the hand is moved clockwise more than it is moved counterclockwise, it will eventually reach the expired stop. When it does, the expired output asserts. An integrating timer is superior for this type of application, where the timed parameter can be on the edge of the band limit and the input continuously sets and resets. Integrating timers will eventually time out and initiate a switching operation if the time that the regulated parameter is out of band averages to be greater than the time that the regulated parameter is in band.

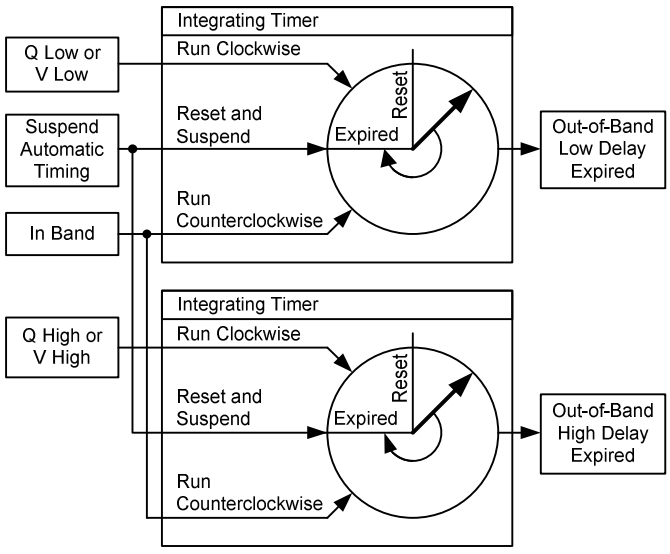

Fig. 9. Integrating timers

There is an overcurrent element that suspends automatic timing when there is a fault on the system. When automatic timing is suspended, the integrating timer registers are reset to zero so that upon release of the timer, they must begin timing again from the reset state before an automatic switching operation can be initiated.

VII. Automatic Switching Logic

The automatic switching logic handles the routing of switching commands to the appropriate capacitor group relays and the monitoring of alarm conditions.

A. Sequencing Logic

To even the number of switching operations between capacitor group relays, the control uses a FIFO sequencing algorithm. The add capacitor sequencing logic will be used to illustrate the scheme.

Referring to Fig. 10, when the control sends an add capacitor command to a capacitor group relay, it sets a nonvolatile latch to record which capacitor group was last added. It then sets the priority of that capacitor group to one and sets the next highest numbered capacitor group to eight, with the remaining capacitor groups set to progressively lower priorities with the numbers wrapping around. In the example shown in Fig. 10, Capacitor Group 3 was the last to receive an add capacitor switching command.

The control then makes the following checks for each capacitor group relay:

- Is the capacitor group enabled in the system?
- Is there good communication to that capacitor group relay?
- Is the capacitor group relay reporting that it has at least one capacitor bank available to add?

For those capacitor group relays that do not pass these three conditions, the priority number is set to zero. In the example shown in Fig. 10, Capacitor Group 5 through Capacitor Group 8 are not enabled in the scheme. Capacitor Group 2 is reporting that it has no capacitor banks available to add. The control then determines which capacitor group has the highest priority number. The next time the control needs to add a capacitor bank, it will send the command to that capacitor group relay. Similar logic is used to determine the next capacitor group to be removed.

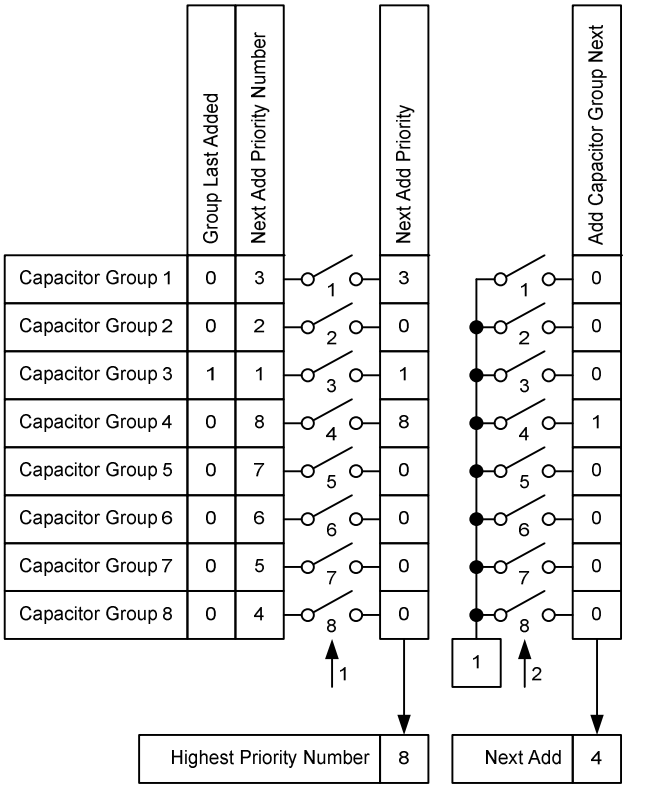

Fig. 10. Add capacitor sequencing logic

B. Switching Logic

Once the integrating timer has called for a capacitor bank to be added or removed, it sends a capacitor switching command to the capacitor group relay with the highest priority to add or remove a cap bank. The command is sealed in until the capacitor group relay indicates that it has started the switching operation by asserting its Switch Op In Process bit.

The control also starts a timer to wait for this feedback from the capacitor group relay. If the timer expires, it sets a fail to start alarm for that capacitor group relay and proceeds to the next capacitor group in the sequence. The alarm condition does not take that capacitor group out of the sequence. When its number comes up again, the control will again send a command to that group.

When the switching command ends (either by a fail to start or deassertion of the Switch Op In Process bit from the capacitor group relay), the time between steps timer delays the next step. When the time between steps timer expires, the logic updates the ΔV and ΔQ registers. It then checks to see if the condition that caused the switching operation has been satisfied. If not, it initiates additional switching operations until it is satisfied. It is not necessary for the integrating timers to time again.

C. Maximum Operations Per Hour (Anti-Hunting) Logic

This function increments a counter register each time a switching operation occurs, as shown in Fig. 11. The user can set a limit on the number of switching operations that are allowed in an hour before an alarm asserts. Every ten minutes, the counter register is decremented by one-sixth of this setting. If the counter register exceeds the threshold, the maximum operations per hour alarm asserts. If the user has enabled the suspend control timer when the maximum operations alarm is asserted function, the integrating timers are blocked and reset until the next ten-minute interval has passed, and the timer is decremented to below the threshold.

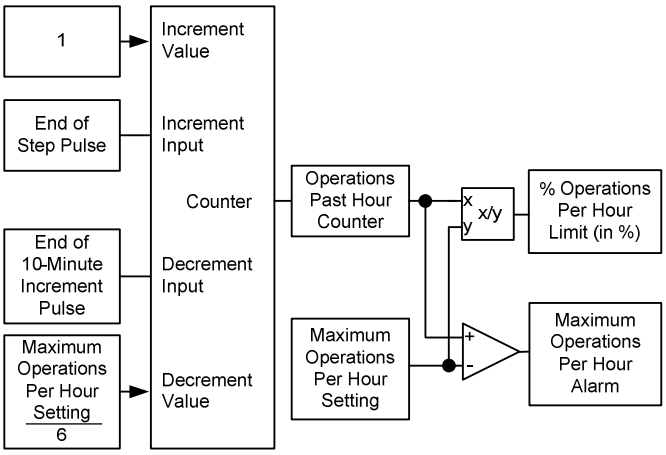

Fig. 11. Maximum operations per hour alarm

VIII. Dead Collector Bus Logic

If the voltage on a collector bus is below a user-settable dead threshold or the tie circuit breaker has opened, the control sends a trip command to each capacitor group relay connected to the dead bus after a user-settable time delay. The capacitor group relay opens the capacitor group main circuit breaker when this command is asserted. The command seals itself in until the bus voltage exceeds the user-settable live bus threshold for a time delay and the tie circuit breaker is closed.

IX. Overview of Capacitor Group Relay Functions

The capacitor group relay provides protection and control of each capacitor group. Overcurrent and breaker failure protection are used for overall fault protection of the capacitor group. Each individual capacitor bank in the group also includes neutral overvoltage protection and capacitor bank vacuum switch failure.

The capacitor group relays manage automatic add and automatic remove commands from the capacitor control with a FIFO sequencing algorithm similar to that described for the control to even out operations of the capacitor bank vacuum switches. The relay determines if a capacitor bank is available to be added with the following checks:

- Is the capacitor bank enabled in the system?
- Is the capacitor bank in automatic mode?
- Is the capacitor bank open?
- Is the capacitor bank not in alarm?
- Is the capacitor bank discharge after open time delay timed out?

The capacitor group relay also automatically opens the capacitor group main circuit breaker upon receiving a dead bus trip command from the capacitor control. When the capacitor group main breaker opens, it also opens each capacitor bank vacuum switch and puts them in manual mode.

The programming of each of the capacitor group relays is identical. The only difference is in the IEC 61850 protocol settings, which are loaded into the relay from the Ethernet port.

X. Protection Functions

A. Capacitor Group Main Overcurrent Protection

Phase and ground overcurrent protection are provided for the capacitor group. Instantaneous elements with a user-settable definite time delay are provided. For instantaneous operation, this time delay can be set to zero. Inverse timing elements are also provided.

B. Capacitor Group Main Breaker Failure Protection

When the capacitor group main circuit breaker is tripped for an overcurrent function, it initiates breaker failure timing. If the breaker failure timer expires, it initiates backup tripping via a physical output contact that can be used to trip a lockout relay.

C. Capacitor Bank Neutral Overvoltage Protection

Ungrounded, wye-connected capacitor banks are typically made up of several individual capacitors that are connected in parallel. Depending upon the bank voltage rating, several of these parallel strings may also be connected in series. When an individual capacitor in the bank fails, it will create an unbalance that will cause overvoltage on other capacitors in the bank. If the unbalance gets too large, capacitors can fail in a cascading manner. One method for preventing cascading failures is to monitor the amount of unbalance voltage between the ungrounded neutral point of the capacitor bank and ground.

Typically, two levels are used. The first level is set to pick up for the level of unbalance caused by the loss of a single can in the bank. This sets a 59N alarm to alert operations and maintenance personnel so that they can repair it before more cans fail and trip the bank. The second level is set at the level of unbalance that will overstress capacitors in the bank with margin. This level is used to trip the capacitor bank vacuum switch to prevent cascading failures.

D. Capacitor Bank Vacuum Switch Failure Protection

When the 59N trip asserts for a capacitor bank, it trips the capacitor bank vacuum switch. If the operate fail timer for that vacuum switch times out while the 59N trip is still asserted, it trips the capacitor group main circuit breaker.

XI. System Validation

The system operation was verified using a Real Time Digital Simulator manufactured by RTDS Technologies. The RTDS is a digital power system simulator capable of continuous real-time operation. It performs electromagnetic transient simulations with a typical time step in the order of 50 microseconds, utilizing a combination of custom software and hardware. The proprietary operating system used by the real-time digital simulator guarantees "hard real time" during simulations.

An RTDS is an ideal tool for thoroughly designing, studying, and testing protection and control schemes. With a large amount of both digital and analog I/O capabilities, physical protection and control devices can be connected to an RTDS to interact with the simulated power system during closed-loop testing.

The system simulated a wind farm connected to a utility. The simulation used one capacitor bank control (Device 90) connected through an Ethernet channel to two capacitor group relays (Device 51/59N). The two capacitor group relays were connected to two separate collector buses and controlled six three-phase capacitors each. Communication between the capacitor control and capacitor group relays was comprised of GOOSE messaging over the Ethernet channel.

RTDS tests were performed as follows:

- The RTDS was configured to drive three current and eight voltage inputs to the relays with real-time analog output from the system model. These analog signals were directly connected to the relay's internal low-voltage board. Three voltages and three currents were connected to the capacitor group relay, and the remaining five voltages were connected to the capacitor control.
- The RTDS was configured to accept digital outputs from the relays. The relay system trip and close signals were connected in order to provide feedback to the RTDS to open and close breakers and vacuum switches in the simulation, as appropriate. Additional output signals were connected to the RTDS for recording the status of various elements for analysis purposes.
- The RTDS was configured to provide circuit breaker and vacuum switch contact indication (52a) to the relays.
- Various system conditions were simulated by adjusting the voltage and power angle of the equivalent utility and wind farm sources. Special emphasis was made to verify proper operation in all four PQ-plane quadrants during both low and high power flow conditions. Boundary conditions, where the two control parameters were in conflict, were verified to ensure that the control would not hunt under those conditions.

XII. Design Documentation

The engineers applying the system wanted it to be easily configurable so that it could be deployed in support of many varied wind farm projects. They did not want to return to the custom control system designers to have the system configured for variations in each project. The requirements specification included a dedicated instruction manual for the system, detailed logic diagrams, and a custom GUI for setting up each device.

Protective relays with powerful programmable logic were used to run the protection and control algorithms. Since most of the protection and control functions were implemented in custom programming, the factory instruction manuals were completely inadequate to describe the system.

The design documentation package included detailed logic diagrams that documented the detailed programming of the control and relay. However, these logic diagrams contained a level of detail required to build the system. This level of detail is too great for the end user applying the device. For this reason, the instruction manual that was provided distilled each function down to text—supplemented with more easily followed functional block diagrams.

Each of the powerful, programmable relays used to implement the VAR control and the capacitor group relay includes thousands of settings. Most of these settings are for functions unused in the capacitor control and the capacitor group relay functionality. And most of the functions that were implemented to provide the functionality required settings that are not covered by the standard functions of the devices. So, it was necessary to build a custom GUI to manage the settings for each device.

Fig. 12 shows a screen shot of the custom GUI that was developed for the control. A similar GUI was developed for the group relay. These software templates work inside the OEM settings software environment. Only the few dozen settings required for the control are visible to the end user that is setting up the control for a specific application. Within the software environment, it is possible to toggle over to the full device settings view if it becomes necessary to modify any of the settings that are not included in the custom interface.

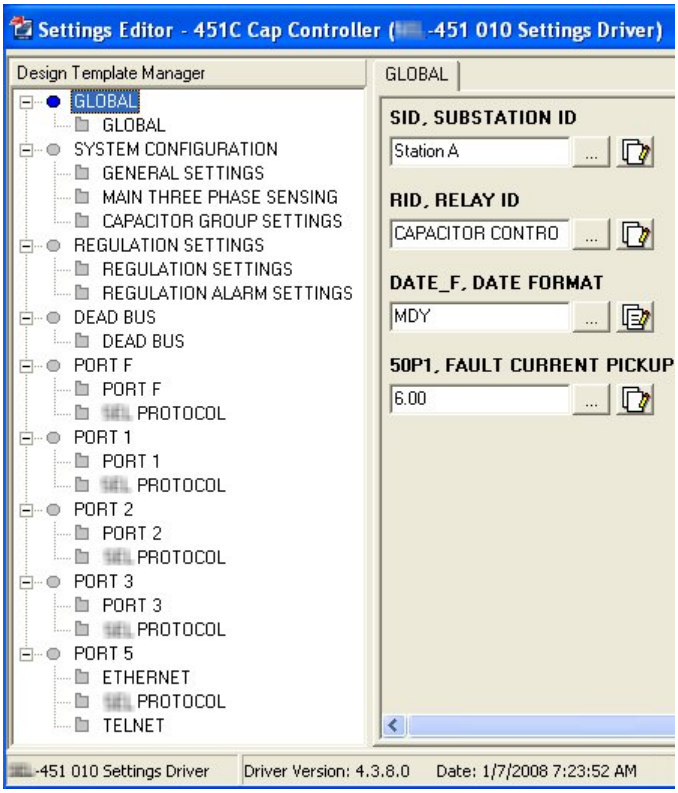

Fig. 12. Settings template for Device 90

XIII. Summary

IEC 61850 simplified the signaling between devices and made the system easily scalable. Other technologies were considered, such as serial communications protocols in a star topology using a logic processor as a communications hub. But the payload and multicast capability of GOOSE messaging made it easy for the central capacitor controller to communicate with many capacitor group relays. This made the system easily scalable to up to eight capacitor groups. No custom configuration is required except to set the number of groups that are enabled in the capacitor controller.

In the capacitor group relays, the only thing that differentiates one capacitor group relay from another is to program a unique IP address into the relay and then choose from one of eight preconfigured IEC 61850 GOOSE message configuration files to load into the Ethernet processor card. Each Ethernet card configuration file maps the GOOSE message bits to the correct logic bits in the receiving control or relay.

Reactive power control has many challenges that were overcome in this project:

- There is not a direct relationship between the controlled parameter and the regulated parameters.
- The controlled quantity's (Q's) effect on the regulated quantities (PF and V) depends upon system conditions.
- Regulating multiple parameters can cause hunting when system conditions result in the two parameters being in conflict.
- The correct control response is dependent upon which quadrant of the PQ plane the system is operating in.

Adaptive algorithms were developed to deal with these challenges. The expected ΔV is calculated by measuring the ΔV from the most recent six switching operations and averaging the measurements. Thus, if system conditions change, the expected ΔV from switching a capacitor bank that is used in the control algorithms will very shortly adapt to the new conditions. Since the VAR supply available from a capacitor bank varies by the square of the terminal voltage, the control measures the bus voltage and calculates the expected ΔQ from switching a capacitor bank for use in the control algorithms.

Devices with powerful programmable logic that perform math calculations in addition to normal Boolean logic functions allowed the development of sophisticated adaptive control algorithms. Use of an RTDS was critical to validating the new control algorithms and the many lines of programmable logic code that had to be developed to implement the system.

The fully programmable HMI on the devices includes programmable LEDs, pushbuttons, an LCD display, and configurable labels. This is a critical feature required to gain acceptance by the end users. Critical features required to gain acceptance by the engineers applying the control system were the custom GUI settings software template that hides thousands of unused settings in the devices and organizes all of the custom function settings, along with a complete design documentation package and instruction manual.

The system has been placed in service at a number of wind farms since it was first developed. The detailed sequence of events reporting capabilities included in the relays have been useful in troubleshooting the few installation and operating problems that have occurred.

XIV. Biographies

Michael Thompson received his BS, magna cum laude, from Bradley University in 1981 and an MBA from Eastern Illinois University in 1991. He has broad experience in the field of power system operations and protection. Upon graduating, he served nearly 15 years at Central Illinois Public Service (now AMEREN), where he worked in distribution and substation field engineering before taking over responsibility for system protection engineering. Prior to joining Schweitzer Engineering Laboratories, Inc. in 2001, he was involved in the development of a number of numerical protective relays. He is a senior member of the IEEE and a main committee member of the IEEE PES Power System Relaying Committee. Michael is a registered professional engineer in the States of Washington, California, and Illinois and holds a number of patents associated with power system protection and control.

Dale Kopf received his BSEE, summa cum laude, from the University of Idaho in 1995 and an MSEE from the University of Idaho in 2000. He has broad experience in the field of electrical engineering. Upon graduating, he served one year at Micron Technologies, where he worked in their Yield Enhancement Department, and then worked eight years at Hewlett Packard, where he completed environmental and electromagnetic compatibility studies, as well as board level design for high-speed digital circuits. Prior to joining Schweitzer Engineering Laboratories, Inc. (SEL) in 2007, he worked for a small consulting firm, where he completed protection studies, relay settings, and installation of a product that used SEL relays. He is a member of the IEEE. Dale is a registered professional engineer in the States of Idaho and California and holds four patents with Hewlett Packard.