Design of a Centralized Substation Synchronizing System

Dale Finney, Mangapathirao V. Mynam, Marcos Donolo, and Amy Sinclair
Schweitzer Engineering Laboratories, Inc.

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***Abstract*—Large substations often have complex and dynamic topologies. The voltage available on either side of an open breaker may originate from a number of sources. This has led to the development of centralized systems to carry out synchronism-check functions to synchronize all breakers within the substation. Such a system uses the status of breakers and disconnects to identify a voltage source for each side of the breaker that is to be synchronized. Custom logic is required to accommodate the topology of a particular substation. In the past, these systems have been realized using custom hardware or programmable logic controllers (PLCs) and significant amounts of wiring. This paper describes in detail a synchrophasor-based approach that provides a significant reduction in the effort and cost required to design, build, and test a centralized synchronizing system. Phasor measurement and control units (PMCUs) transmit voltage phasors and breaker and disconnect status to a central controller. The central controller time-aligns the data and selects the correct voltages to use for synchronizing according to the present status of the breakers and disconnects. Once the appropriate checks of the voltages are made, a close command is sent from the central controller to the PMCU responsible for the breaker that is to be closed. A primary objective is to reduce the requirement for custom logic as much as possible. The design relies heavily on using the program organizational units (POUs) described in IEC 61131. These can be developed, tested, write-protected by passwords, and easily reused in subsequent projects.**

The synchrophasor-based approach proposed in this paper is also applicable when synchronizing two power sources. This usually entails controlling voltage magnitude and frequency in one island, whereas synchronism check does not carry out voltage or frequency control. The scheme described in this paper is applicable to synchronism check and can be extended to support synchronizing two islands.

I. Introduction

This paper describes the implementation of a centralized synchronizing scheme for substations with complex topologies. Substation configurations exist that present challenges for synchronizing. One such configuration is shown in Fig. 1. Assume that Breaker 2 is to be closed. A synchronizing voltage source for the top of Breaker 2 is provided by Potential Transformer A (PT A) when Breaker 1 is closed and by PT B if Disconnect 4 is closed. A similar situation exists for sources on the bottom of Breaker 2. A distributed scheme can be implemented with a dedicated synchronism-check device for each breaker. In this case, each device needs to select the voltage source from four sources based on breaker and disconnect status. The logic for the voltage selection is unique for each breaker.

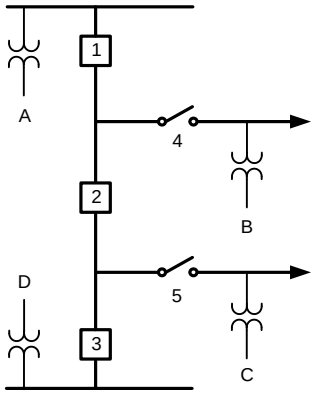

Fig. 1. Substation Showing Available Synchronizing Sources

Complexity can be reduced by adding or relocating PTs. For instance, in Fig. 1, if PT B and PT C were moved to the left-hand sides of Disconnect 4 and Disconnect 5, respectively, then the need for voltage selection logic would be eliminated. However, it is not always practical to place PTs in the optimum location for synchronizing. For instance, placing a PT on a gas-insulated switchgear (GIS) bus is likely to be more expensive than placing it at the line terminal air-to-gas bushing.

It is possible to implement a distributed scheme wherein an intelligent electronic device (IED) is dedicated to synchronizing each breaker. Each IED would either have to measure voltages from all required PTs (often not possible) or switch PTs externally. The wiring and logic associated with each distributed scheme when taken as a whole would likely be more complex than a centralized scheme.

II. Conventional Centralized Synchronizing Scheme

Centralized schemes have been implemented to address the issue described previously. Conventional implementations are composed of two main modules, as shown in Fig. 2.

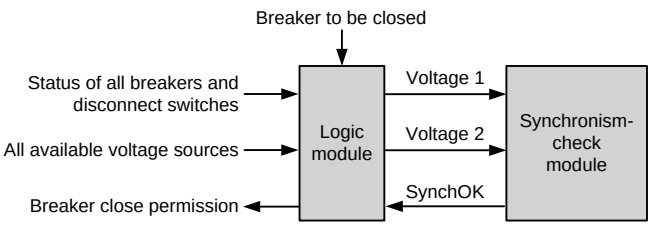

Fig. 2. Block Diagram of Centralized Synchronizing Scheme

The logic module performs voltage selection. Depending on the breaker to be closed, the logic module selects two voltage measurements (Voltage 1 and Voltage 2) and passes them to the synchronism-check module. The synchronism-check module sends a *SynchOK* signal back to the logic module if the conditions for synchronism check are met. The logic module then routes a close permission to the particular breaker to be closed.

In present implementations, both modules have been implemented using custom hardware. The scheme could also be implemented using an off-the-shelf programmable logic controller (PLC) and a synchronism-check relay.

The advantage of a centralized scheme is that it concentrates the hardware and associated logic functionality in one location. A disadvantage is the significant amount of wiring required to bring all of the voltage and status signals to a central location. In implementations where a supervisory control and data acquisition (SCADA) control to close the breaker is provided by a central remote terminal unit (RTU), the synchronizing scheme could be located in the same cabinet. Because the RTU usually requires the same signals as the synchronizing scheme, this allows signals to be shared.

Another disadvantage of the centralized scheme is that a single point of failure impacts the synchronizing capability of the entire substation.

III. Synchrophasor-Based Control

Time-synchronized phasor measurements, also known as synchrophasors [1], have been widely used for visualization and postmortem applications such as power system model validation [2] [3]. Phasor measurement and control units (PMCUs) provide the synchronized measurements. These time-synchronized measurements, complemented with the advent of synchrophasor-based controllers (SBCs), allow users to implement closed-loop synchrophasor-based control schemes.

Closed-loop control schemes using synchrophasors have been applied in the power system. Some of the implementations in service today are the following:

- Islanding detection in distributed generation (DG) applications uses phase angle measurements at the DG location and the point of common coupling and calculates the rate of change of angle difference (slip) and the rate of change of slip [4].
- Remedial action scheme based on low-frequency oscillations uses the power measurements from two intertie transmission lines and measures the low-frequency oscillations. The scheme sends a command to disconnect the intertie connection when the oscillations are associated with negative damping [5].

SBCs mainly provide the following functions: time alignment (TA), built-in logic functions, and user-programmable logic functions.

A. Time Alignment

Time alignment is a key function in the design of synchrophasor data concentrators and controllers. It allows for communications latencies between the phasor measurement units (PMUs) and the controller or data concentrator. The measurements are time-tagged with a common time reference (typically Global Positioning System [GPS]). The TA function opens a time window (message wait time) where it expects all the measurements with the same time tag to arrive, independent of their location. Some implementations force the device measurements that arrive outside the message wait time to zero and flag these measurements to represent bad quality. This wait time is typically configurable and should be set based on the communications latencies and applications. For example, a smaller message wait time is applicable for closed-loop control applications, whereas for postmortem or data archiving applications, a longer message wait time may be acceptable.

B. Built-In Logic Functions

Specifically for SBCs, the capability to perform calculations or mathematical operations on the time-aligned phasor measurements is critical. Additionally, more advanced built-in functions are made available in some controllers, and some of these functions include the following:

- Three-phase real and reactive power
- Phase angle difference
- Modal analysis
- Substation state and topology processor (SSTP), as described in Subsection B of Section IV

Processing the available logic functions at deterministic low computation times is another key requirement for SBCs, as it is for any controller. Today, SBCs are available that can achieve computation times in the order of 4 milliseconds. The low processing time of the controllers allows the implementation of closed-loop synchrophasor-based control schemes that require strict response times (in the order of 100 milliseconds). Based on the output of the control schemes, SBCs are capable of sending a control command to the appropriate device to take a control action. In some implementations, the PMCUs provide synchrophasor measurements and are capable of receiving the control commands from the SBCs and taking appropriate action. Fig. 3 shows the potential latencies that are involved in a synchrophasor-based control scheme. Users must compare these latencies with the timing requirements of the application for any critical control scheme using synchrophasors.

Fig. 3. Processing Latencies

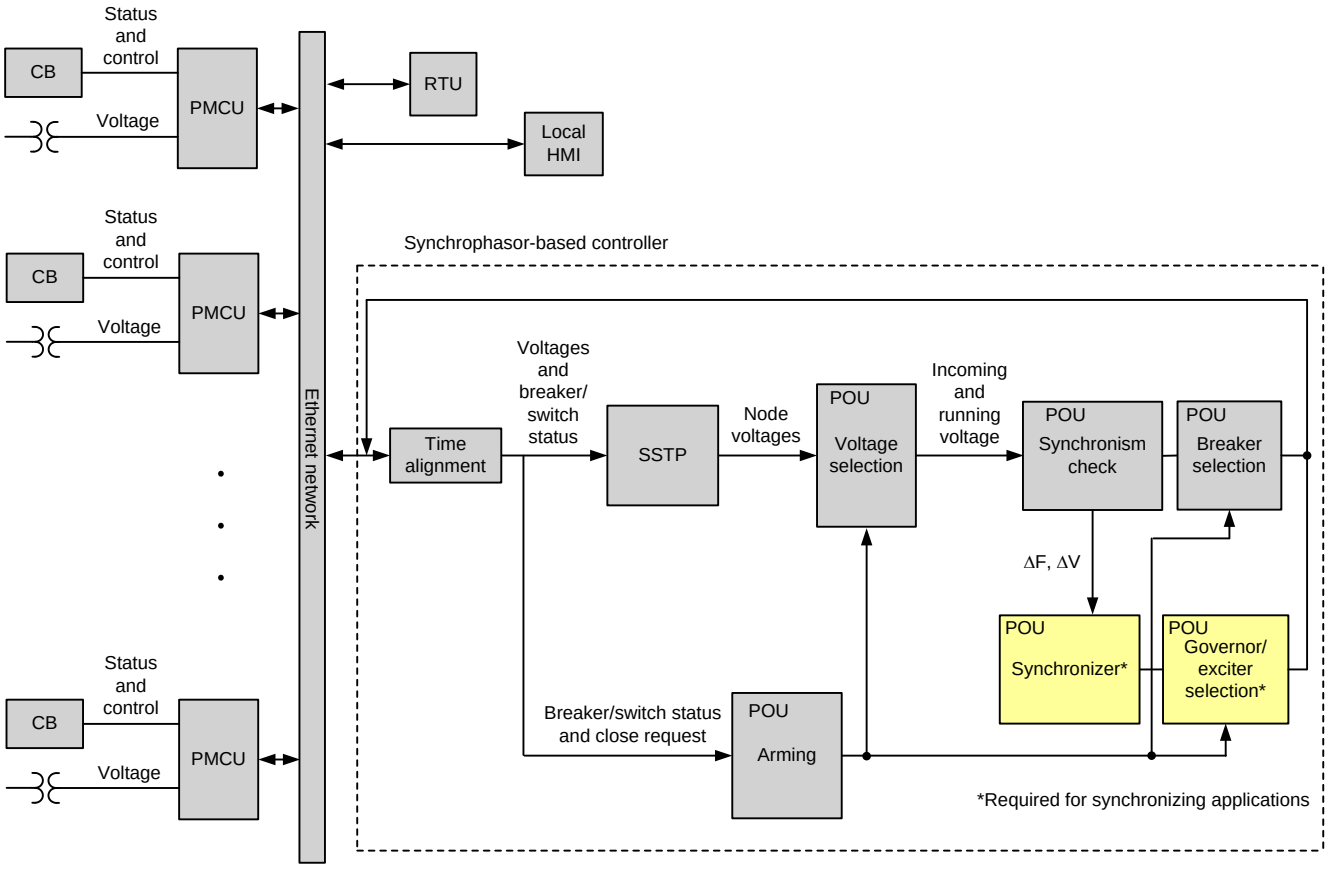

Fig. 4. Synchrophasor-Based Centralized Synchronizing System

C. User-Programmable Logic Functions

Some of the SBCs available today provide users with IEC 61131-3-compatible support for multiple programming languages [6]. These languages include the following:

- Structured text (ST)
- Function block diagram (FBD)
- Ladder diagram (LD)
- Continuous function chart (CFC)
- Instruction list (IL)

The standard provides the syntax and semantics for the programming languages. Depending on user familiarity with a particular language and the complexity of the program, users can choose a particular programming language.

IV. Centralized Synchronizing System Using Synchrophasors

The system shown in Fig. 4 consists of PMCUs, an Ethernet network, and a central SBC. The SBC consists of two functions that are built-in features (time alignment and an SSTP) and several program organizational units (POUs) that have been constructed using IEC 61131 programming languages.

PMCUs located in each bay are responsible for measuring the voltage and frequency and transmitting synchrophasors to the SBC. Note that in Fig. 4, each voltage source has a dedicated PMCU. Connecting multiple voltage sources to the same PMCU requires a PMCU that can measure multiple frequencies. PMCUs are also responsible for sending breaker and disconnect status and receiving close commands.

Using the time alignment of the data from multiple PMCUs, the SSTP module constructs the topology of the substation based on the user configuration and the existing state of the breakers and disconnects.

When a user chooses a particular breaker to be closed, the voltage selection block selects incoming and running voltages for synchronization using the present topology. One key advantage of this system is the capability to select the best available voltage measurements based on the topology of the system as determined by the SSTP to run the synchronizing logic. The synchronism-check module checks that the incoming and running sources are in phase and that the magnitudes and frequencies of the two sources are within limits (typically close to nominal). The scheme then generates the close command, which is routed to the breaker that is to be closed.

The SBC can receive synchrophasor data at up to 60 messages per second. The SBC can process logic at rates of up to 240 Hz or four times per cycle at 60 Hz. In a synchronizing application, for a maximum slip of 0.067 Hz, as specified by IEEE C50.12 and IEEE C50.13 [7] [8], a 240 Hz processing rate equates to a shift of 0.1 degree per logic scan. Thus, 100 milliseconds of latency represents 24 logic scans at 0.1 degrees of travel per scan, which is 2.4 degrees of error in the actual angle difference. In applications where synchronizing is carried out at a much higher slip rate, the

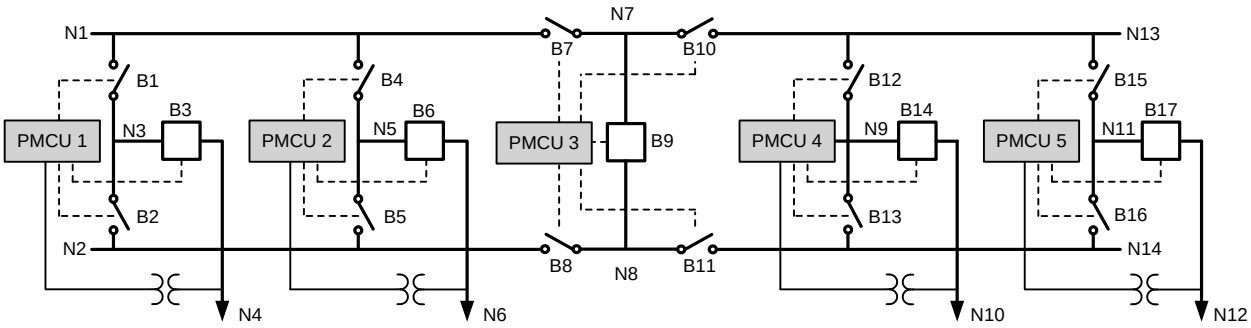

Fig. 5. Example Substation

additional latencies introduced by this scheme could hinder performance [9].

The example substation shown in Fig. 5 is used to describe the new scheme. In this substation, PTs are located only at the line terminals. Each line terminal can be connected to either bus. Buses can be sectionalized using disconnect switches.

The controller logic is subdivided into several modules, which are described in the following subsections.

A. Time Alignment

Time alignment is described in detail in Section III. It is carried out automatically and ensures that all downstream operations are made using time-coherent measurements.

B. Substation State and Topology Processor

The SSTP gathers time-aligned synchrophasor data along with the status of breakers and disconnect switches from PMUs and PMCUs for substation state and topology assessment. The SSTP uses these data to identify measurement errors and improve measurement accuracy.

1) SSTP Structure

The SSTP module is organized into three main processors (see Fig. 6): the topology processor (TP); the current processor (CP), which is not used for this application; and the voltage processor (VP). The topology processor processes breaker and disconnect switch status to obtain the substation topology and then makes this information available to the current and voltage processors. The current and voltage processors use the substation topology and the synchrophasor data to detect measurement errors and refine the current and voltage measurements in real time.

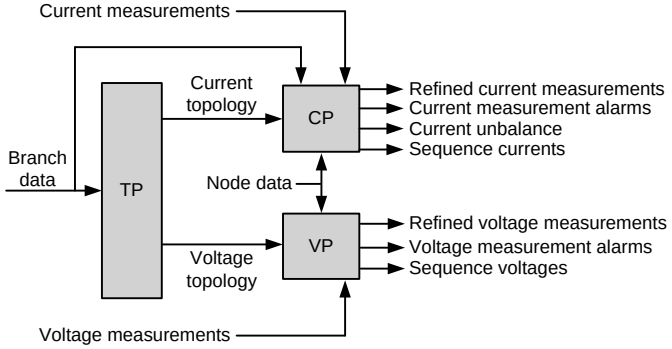

Fig. 6. SSTP Includes Topology, Current, and Voltage Processors to Refine Measurements and Identify Measurement Errors

Referring to Fig. 5, assume we are trying to synchronize Node N4 to the rest of the substation through Breaker B3. The incoming voltage is measured by the PT at Node N4, and for the running voltage, the SSTP takes the median of the voltages measured at Nodes N6, N10, and N12. If one of the voltage measurements is bad (e.g., the PT fuse has failed), the median discards the bad measurement, making the synchronizer more robust than when using traditional methods. Note that averaging the two good voltage measurements with a bad measurement will not produce a quantity suitable for synchronization.

The topology processor uses branch status information to provide topology information for the current processor (not used in this application) and the voltage processor. The topology processor determines the current topology and the voltage topology by merging busbar nodes to create node groups according to the closed status of the branches in the busbar arrangement. To create the current topology, the topology processor merges nodes when the nonmetered branches are closed or when the branch close status quality of the nonmetered branch is false. To create the voltage topology, the topology processor merges nodes when branches are closed. The current processor uses the current topology for current measurement checks and refinement. The voltage processor uses the voltage topology for voltage measurement checks and refinement.

2) Node Merging Process Example

As stated previously, the topology processor uses branch status to merge nodes. This allows node voltages to be combined. To illustrate the node merging process, consider Fig. 5. The bus arrangement has 14 nodes numbered N1 to N14 and 17 branches numbered B1 to B17 in Fig. 5. There are five metered branches (B3, B6, B9, B14, and B17). Only Nodes N4, N6, N10, and N12 include voltage measurements. The topology processor considers all branches as merging branches to create the voltage node groups. Table I shows the branch-to-node data array for the voltage processor when all branches are open. The array shows the *From* and *To* node identification for each branch.

TABLE I
BRANCH-TO-NODE DATA ARRAY FOR THE TOPOLOGY PROCESSOR WHEN ALL BRANCHES ARE OPEN

	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15	B16	B17
From	1	2	3	1	2	5	1	2	7	7	8	9	9	9	11	11	11
To	3	3	4	5	5	6	7	8	8	13	14	13	14	10	13	14	12

TABLE II
BRANCH-TO-NODE DATA ARRAY FOR THE VOLTAGE PROCESSOR WHEN BRANCH 2 MERGES NODE 2 AND NODE 3

	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15	B16	B17
From	1	2	2	1	2	5	1	2	7	7	8	9	9	9	11	11	11
To	2	2	4	5	5	6	7	8	8	13	14	13	14	10	13	14	12

After a branch closes, the topology processor replaces all instances of the *To* node ID with the *From* node ID in the branch-to-node data array. For example, Table II shows the new array after Branch 2 merges Node 2 and Node 3. In this case, the *To* node ID is 3 and the *From* node ID is 2, as shown in Table I. In Fig. 5, Branch 2 is connected from N2 to N3. Thus, when Branch 2 closes, all entries that were a 3 in Table I become a 2 in Table II (highlighted in yellow).

When this topology is passed to the voltage processor, it combines the voltage measurements available at both Node 2 and Node 3. No other voltage measurements are combined.

Without the SSTP, custom logic would be required to determine the voltages on either side of a breaker. For example, the pseudo code in Fig. 7 presents the logic required to determine the voltage at N3 in Fig. 5 (the running voltage needed to synchronize B3).

```
(* voltage at N3 *)
IF
   B6=ON and ((B1=ON and B4=ON) or (B2=ON and B5=ON))
THEN
       VR:=N6;
ELSEIF
   B14=ON and ((B1=ON and B7=ON and ((B10=ON and B12=ON)
   or (B9=ON and B11=ON and B13=ON)) or (B2=ON and B8=ON
   and ((B11=ON and B13=ON) or (B9=ON and B10=ON and
   B12=ON)))
THEN
       VR:=N10;
ELSEIF
  B17=ON and ((B1=ON and B7=ON and ((B10=ON and B15=ON)
  or (B9=ON and B11=ON and B16=ON)) or (B2=ON and B8=ON
  and ((B11=ON and B16=ON) or (B9=ON and B10=ON and
  B15=ON)))
THEN
      VR:=N12;
ELSE
      VR:=0;
```

Fig. 7. Custom Logic Required for N3 if the SSTP Is Not Used

Unique logic would be required for each of the breakers, and this logic would be specific to the particular substation.

The SSTP logic can also be used as a front end to a load-shedding logic application, where a particular load can be automatically selected to be shed based on the dynamically changing topology.

C. Arming Logic

Referring once again to Fig. 4, the arming logic processes close requests. The logic, shown in Fig. 8, is responsible for opening a window for synchronizing and for rejecting close requests if synchronizing is in progress on another breaker.

The arming logic resets after a fixed delay (30 seconds in this example). In a practical implementation, this logic may also be subject to site-specific requirements regarding situations such as failed close attempts or station-wide interlocks.

For our example substation, a PMCU is dedicated to each breaker in Fig. 5. The output of the logic, CB_TO_CLOSE, is a number ranging from 0 to 5 that indicates the breaker to be closed.

In this example, close requests originate from the PMCU associated with a particular breaker but could also originate from another source such as an RTU or local human-machine interface (HMI).

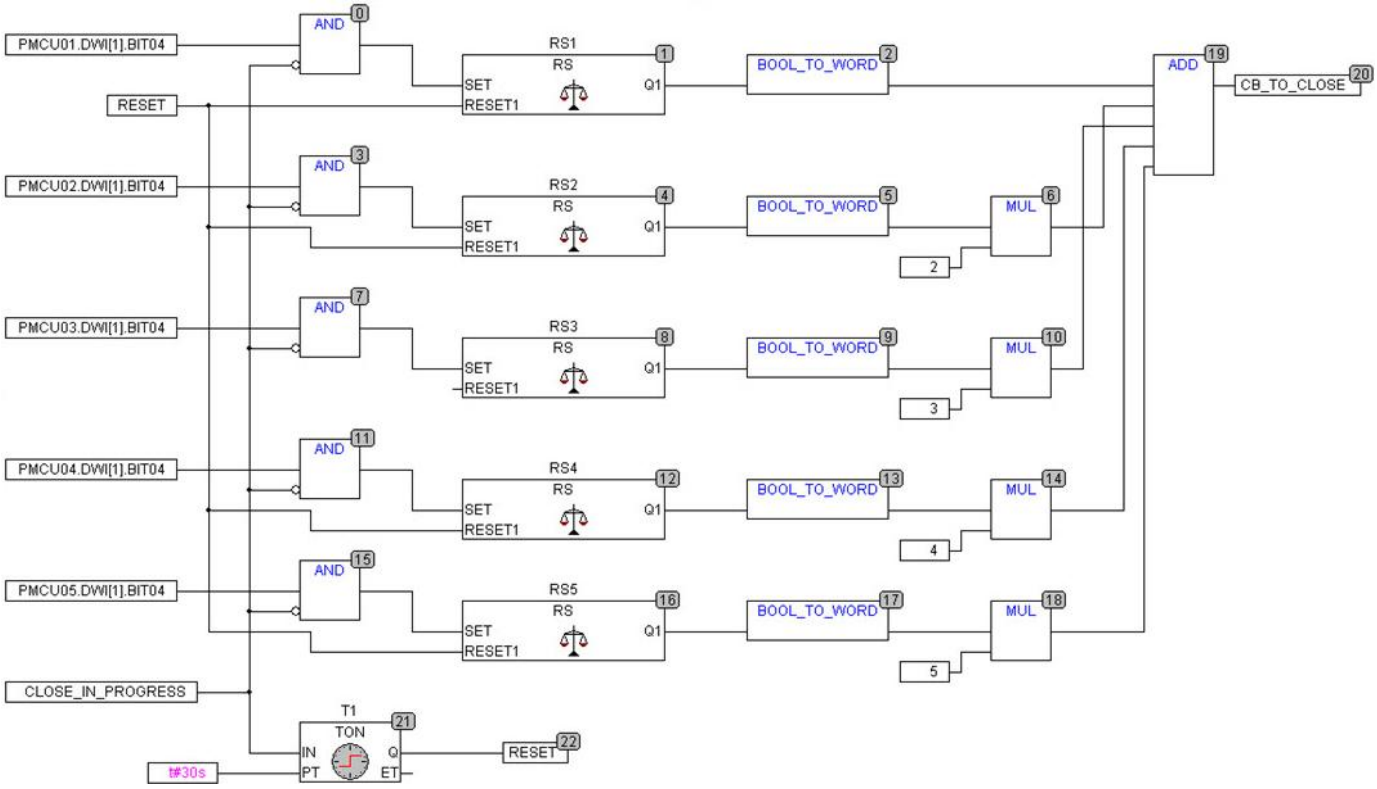

Fig. 8. Arming Logic

```
0001 PROGRAM VOLT_SELECT
0002 VAR
0003     NI: INT; (* Incoming voltage node*)
0004     NR: INT; (* Running voltage node *)
0005 END_VAR
0006
0007
0008
```

```
0001
0002 NI:=MUX(CB_TO_CLOSE,0, 4, 6, 8, 10, 12); (* select incoming node *)
0003 NR:=MUX(CB_TO_CLOSE,0, 3, 5, 7, 9, 11); (* select running node *)
0004
0005 IF NI <> 0 THEN
0006     VI_Mag := SSTP_OUT.list_of_nodes.node[NI].A_phase.scaled_voltage_measurement[1].mag;     (* Incoming voltage magnitude *)
0007     VI_Ang := SSTP_OUT.list_of_nodes.node[NI].A_phase.scaled_voltage_measurement[1].ang;     (* Incoming voltage angle *)
0008     VR_Mag := SSTP_OUT.list_of_nodes.node[NR].A_phase.scaled_voltage_measurement[1].mag; (* Running voltage magnitude *)
0009     VR_Ang := SSTP_OUT.list_of_nodes.node[NR].A_phase.scaled_voltage_measurement[1].ang;   (* Running voltage angle *)
0010 ELSE
0011     VI_Mag:=0;
0012     VI_Ang:=0;
0013     VR_Mag:=0;
0014     VR_Ang:=0;
0015 END_IF
```

Fig. 9. Voltage Selection Logic

D. Voltage Selection Logic

The voltage selection logic chooses the incoming and running voltages for the particular breaker to be closed. This logic is shown in Fig. 9. The IEC 61131 ST programming language is chosen for this module because it is more appropriate for this application. Note that this logic is very simple because it is receiving the node voltages from the SSTP. The nodes on either side of a breaker are always the same. For example, if Breaker B3 is to be closed (CB_TO_CLOSE=1), then the node for the incoming voltage (NI) is N4 and the node for the running voltage (NR) is N3. N4 has a physically connected voltage source. On the other hand, N3 does not have a physically connected voltage source but derives its voltage through the process of node merging.

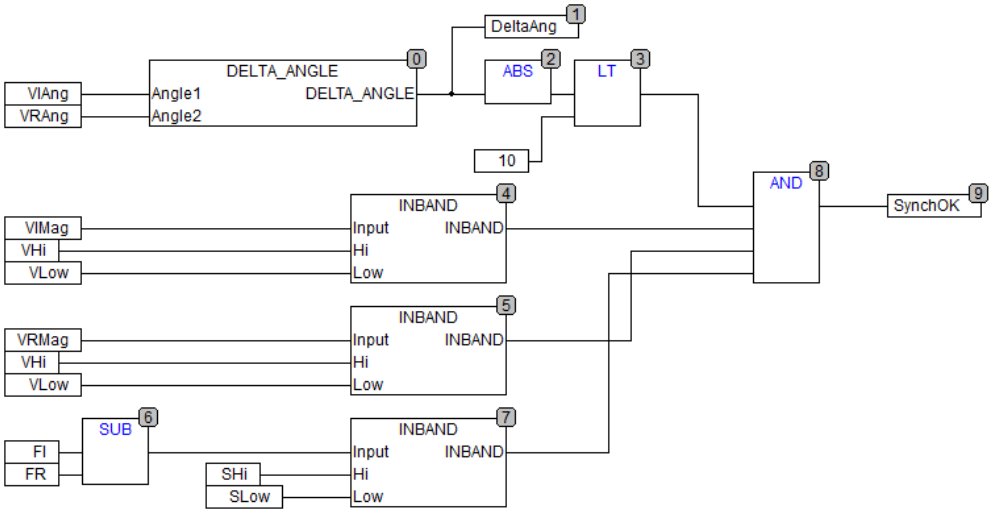

Fig. 10. Synchronism-Check Logic

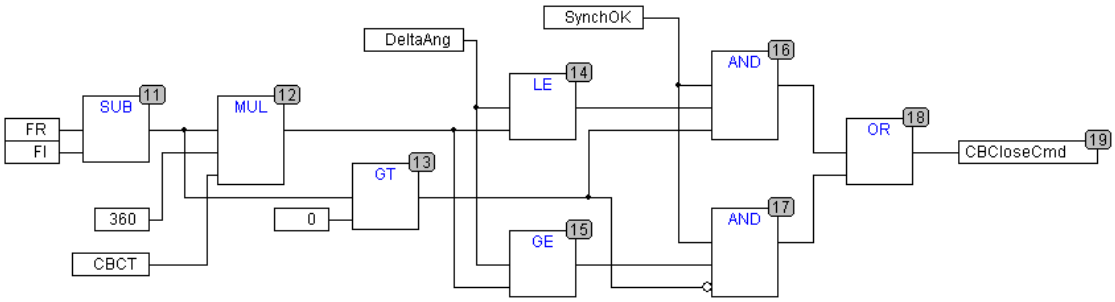

Fig. 11. Time-Advanced Closing Logic

E. Synchronism-Check Logic

The synchronism-check logic shown in Fig. 10 receives the incoming and running voltages and checks that the difference in angle, magnitude, and frequency is within limits. The first input to the AND gate asserts when the absolute angle between the incoming and running voltages is less than a pickup threshold (10 degrees in this example). The remaining three inputs to the AND gate assert when the magnitudes and slip of the incoming and running voltages are within a set band. If the limits are satisfied, the logic gives permission (SynchOK) to the close command logic. In Fig. 10, an additional logic function (INBAND) has been developed to further streamline the logic.

The closing logic is shown in Fig. 11. This logic includes a feature to provide a time-advanced close command based on angle difference and slip frequency and the circuit breaker close time. First, slip is calculated by subtracting the incoming and running frequencies. The advance angle is equal to slip • 360 • CBCT (circuit breaker close time in seconds). This angle is compared with the actual angle between the two sources (DeltaAng). The comparison is less than or greater than, depending on whether the slip is positive or negative. Accounting for circuit breaker close time ensures that angle difference is minimized at the instant the breaker primary contacts close.

Although intended to address circuit breaker delays, this feature could also be used to accommodate other sources of delay.

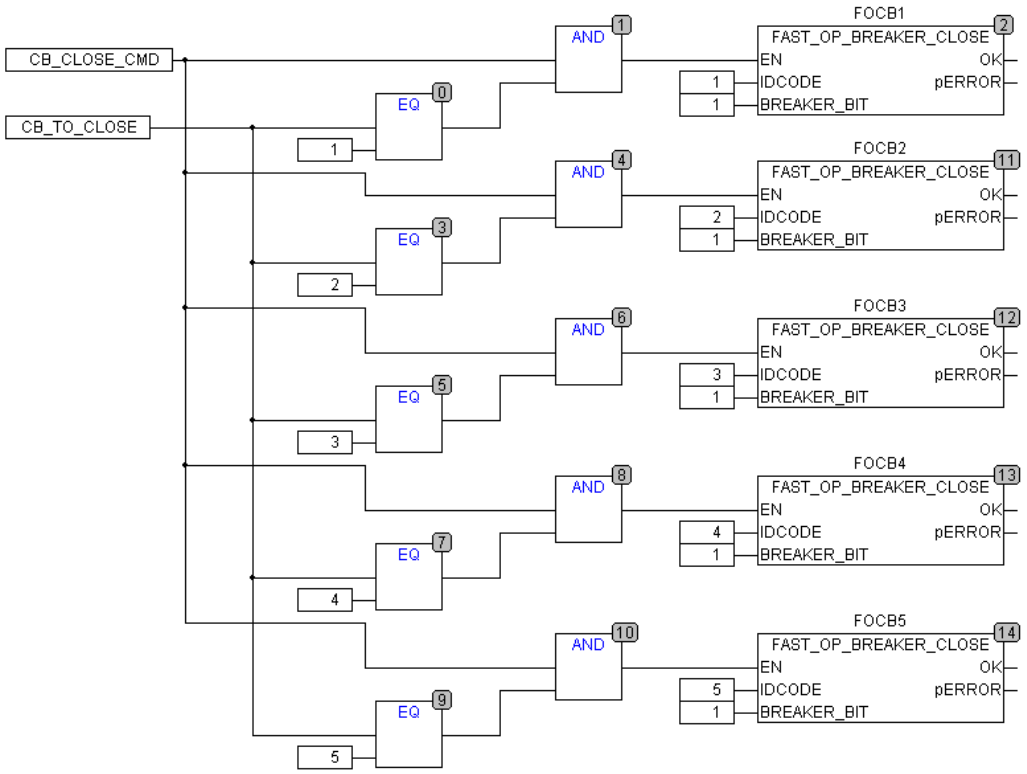

Fig. 12. Close Selection Logic

F. Breaker Selection Logic

The breaker selection logic routes the close command to a particular breaker, as shown in Fig. 12.

As mentioned at the beginning of this paper, the scheme is applicable both to synchronism check and synchronizing. In a synchronizing scheme, similar selection logic would also route raise/lower commands (not shown) to particular generator controls in the same manner. A PMCU would be located at the generator controls in this case to translate raise/lower commands to electrical contact closures.

V. Advantages

The proposed scheme has significant advantages over the conventional scheme described in Section II. All signals are exchanged over the substation local-area network (LAN), so most hard-wired connections disappear. Today, many modern protective relays support synchrophasors and are wired to all of the voltage sources throughout the substation. These same relays are also often wired with breaker and switch status throughout the substation. Thus, in substations where relays supporting synchrophasors are applied, the need for additional hardware and wiring is minimal. A redundant LAN architecture coupled to redundant central controllers removes single points of failure. The proposed scheme can more easily be applied than a hard-wired scheme in locations where voltage sources and breakers are separated by long distances, such as the case of a generator power house that connects to the grid through a remote switchyard.

The proposed scheme can be designed for easy modification and maintenance. The scheme logic can be initially designed taking into consideration the ultimate size of the substation. The logic intended for future devices would initially be unassigned. If the substation were subsequently extended to include a new circuit and associated breakers, then a PMCU could be added to include new voltage and status signals. These new signals would be routed to the SBC and assigned to unused logic inputs. Changes would be required for the SSTP; however, configuration of this module is more akin to setting a protection function than to developing logic. Most logic modules would require no modification. These modules can be locked against editing after initial design and testing.

The features described in this paper also make this scheme easily adaptable to a different substation with a different topology. Most of the effort is restricted to configuration of the SSTP.

The SSTP also improves the quality of the voltage measurements. When several voltage sources are connected to a node, the SSTP calculates the node voltage as the median of the available measurements.

VI. Conclusion

The scheme described in this paper performed as expected during bench testing, showing that it is a viable alternative to existing centralized approaches.

This paper demonstrates that the inherent time-stamping provided by synchrophasor measurements allows them to be effectively applied for critical control functions in the power system.

The approach makes extensive use of IEC 61131 programming features. This results in simpler, more modular code.

In a conventional application, considerable effort would be required to develop the voltage selection logic for each breaker. This logic would be unique for each breaker. If the scheme was reapplied to a different substation, then this logic would have to be rewritten. This paper shows how the SSTP can be used to replace custom logic. Configuration of the SSTP amounts to defining nodes and branches—arguably a much simpler process with less potential for error. This results in applications that are more generic and thus more easily adaptable.

This effort represents a further step in the transition to substation automation designs that leverage advanced IEDs and communication to reduce cost and complexity.

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VIII. Biographies

Dale Finney received his BSEE from Lakehead University and his MSEE from the University of Toronto. He began his career with Ontario Hydro, where he worked as a protection and control engineer. Currently, Mr. Finney is employed as a senior power engineer with Schweitzer Engineering Laboratories, Inc. His areas of interest include generator protection, line protection, and substation automation. Mr. Finney holds several patents and has authored more than 20 papers in the area of power system protection. He is a member of the main committee of the IEEE PSRC, a member of the rotating machinery subcommittee, and a registered professional engineer in the province of Ontario.

Mangapathirao (Venkat) Mynam received his MSEE from the University of Idaho in 2003 and his BE in electrical and electronics engineering from Andhra University College of Engineering, India, in 2000. He joined Schweitzer Engineering Laboratories, Inc. (SEL) in 2003 as an associate protection engineer in the engineering services division. He is presently working as a senior research engineer in SEL research and development. He was selected to participate in the U.S. National Academy of Engineering (NAE) 15th Annual U.S. Frontiers of Engineering Symposium. He is a senior member of IEEE.

Marcos Donolo received his BSEE from Universidad Nacional de Río Cuarto, Argentina, in 2000 and his MSEE (2002), his master of mathematics degree (2005), and his Ph.D. in electrical engineering (2006) from the Virginia Polytechnic Institute and State University. Since 2006, he has been with Schweitzer Engineering Laboratories, Inc., where he is presently a lead research engineer. He is a senior member of IEEE.

Amy Sinclair received her BSEE degree from Queen's University, Kingston, in 1989. She joined Ontario Hydro in 1989, working for ten years as a protection and control engineer in the areas of design, operations, and project management. In 2000, she joined ELECSAR Engineering as a project manager with a focus on protective relaying and substation design. Since December 2006, she has been employed with Schweitzer Engineering Laboratories, Inc. as a field application engineer located in Chatham, Ontario. She has been registered as a Professional Engineer of Ontario since 2001.

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