

New Inrush Stability Algorithm Improves Transformer Protection

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Abstract

This paper presents a transformer protection logic for security during magnetizing inrush conditions, especially under transformer ultrasaturation resulting in low levels of even harmonics in the differential current. The protection scheme includes an inrush unblocking logic to accelerate tripping for internal short circuits. The paper explains key principles, shares implementation details, and illustrates the concepts with simulation results and field cases.

1 Introduction

Large power transformers are key assets in any power system. When damaged, they are expensive and difficult to replace factoring in the cost, manufacturer lead time, and transportation. When a power transformer suffers an internal short circuit, the outcome is primarily driven by how much core damage occurred and whether the tank ruptured. If the tank ruptures due to the pressure buildup caused by a rapid oil decomposition, the repairs, if possible, are typically much more expensive. A tank rupture results in an oil spill, and if the oil containment system is not in place or malfunctions, it may result in environmental damage as costly as the transformer itself. When the tank ruptures, there is an increased danger of an oil fire leading to total destruction of the transformer and potential destruction of its surroundings.

Medium and large transformers are therefore protected against short circuits with differential elements. The differential protection principle in general is very secure, sensitive, and fast. In the case of a power transformer, the differential element follows the ampere-turn balance across the transformer core [1] allowing it to balance currents from galvanically isolated windings through the use of Kirchhoff's current law. As with any typical differential protection element, a transformer differential element (87T) includes a percentage restraint (bias) to cope with current transformer (CT) saturation on external faults [2]. Newer numerical 87T implementations also provide for an external fault detection logic for extra security [1].

Transformers draw a magnetizing inrush current during energization. Inrush is caused by partial cycle saturation of the transformer magnetic core. The magnetizing impedance of the transformer drops significantly during the periods of time when the core is saturated, causing high currents that are unipolar in nature (saturation occurs only on the peaks of the positive or negative half cycles). The magnetizing branch of the

transformer creates an "unmeasured" branch in the 87T differential zone and violates the current balance around the transformer windings. 87T elements see the inrush current as a differential signal with no corresponding through-current restraint. Thus, they are susceptible to tripping during initial energization and – potentially – during a voltage recovery inrush. Percentage restrained differential relays require some means of differentiating between a differential current caused by an inrush and a differential current caused by an internal fault.

Early designs of 87T relays had to deal with the limits of their contemporary technology. Relay designers observed that signals with asymmetrical distortions are rich in even harmonics, and therefore, the unipolar currents caused by inrush should also be rich in even harmonics. Analog filter circuits could easily be built to extract the second- and fourth-harmonic components of the differential current, and these could be used as a surrogate measure for determining if the differential current is due to an internal fault or inrush.

Harmonic-based logic for security during inrush conditions served our industry well, but it is not without limitations. Ultrasaturation of the transformer core results in low harmonic content and threatens 87T security on inrush. Spurious harmonics are created when the differential current develops due to an internal fault, and these spurious harmonics slow down the 87T operation. Saturated CTs produce harmonics in the secondary differential current, jeopardizing both the 87T speed and dependability.

Today, with digital technology, we can design a relay algorithm that detects specific characteristics of inrush. This paper presents waveshape-based algorithms and logic to enhance security during inrush, accelerate tripping times, and improve dependability for internal faults.

2 Harmonic-based solution for transformer differential element security during inrush

Harmonic-based solutions have been used from the onset of 87T relays. Two methods came into common use. In harmonic blocking elements, a comparator circuit determines the ratio of the even-harmonic component to the fundamental component of the differential current and blocks the differential element if the ratio is high. In harmonic restraint elements, the magnitudes of the even harmonics are added to the restraining signal in the percentage restrained comparator to prevent the differential current from overcoming the slope (bias) characteristic. Both of these schemes face challenges, as explained below.

2.1 CT saturation during heavy internal faults

During heavy internal faults, CTs may saturate and generate harmonics in their secondary currents. These harmonics may block or delay operation of an 87T element that uses harmonics for inrush detection. This problem can be addressed by the requirement to select CTs that do not saturate for the time it takes the 87T element to operate (the CT time-to-saturation requirement).

A high-set unrestrained differential element is an alternative solution. We have an option to trip without percentage restraint and harmonic blocking if the differential current is above the highest possible inrush current and the highest possible spurious differential current during external faults. Many 87T relays apply an external fault detection logic to distinguish between external faults and other events. In this case, the unrestrained differential element needs to be set just above the highest possible inrush current.

Because harmonics do not block the unrestrained element, it trips for heavy internal faults, even if CTs saturate and inadvertently block the percentage restrained 87T element.

Yet another solution to CT saturation during internal faults is to use harmonic restraint logic. This logic does not block from harmonics but increases the restraint with harmonics in the differential current. During heavy internal faults, the large differential current overcomes the restraint even if the latter is boosted with spurious harmonics caused by saturated CTs.

2.2 CT saturation during inrush

A typical inrush current is unipolar with a slow decay rate. The unipolar nature of the primary inrush current drives the CT flux in one direction. This unipolar current can be initially as high as several times the transformer nominal current, and it eventually results in CT saturation. Even CTs that are properly sized to handle the maximum fault current and X/R ratio without saturating may saturate on inrush due to this nonsinusoidal unipolar, long duration current. A saturated CT tends to reduce the harmonic ratios in the secondary inrush current, compared with the true primary inrush current, jeopardizing the security of the 87T element. Some 87T elements use cross-phase blocking, and some users may choose to reduce the harmonic blocking thresholds. These solutions may alleviate this problem to a degree, but they do so at the expense of 87T dependability and speed.

2.3 Low harmonic levels during inrush

Newer transformers with high-permeability core steel often experience ultrasaturation during inrush. In ultrasaturation, the flux density is above the knee point of the transformer magnetizing curve (B-H curve [3]) for longer fractions of the power system cycle, and therefore, it experiences much less distortion and lower harmonic content. A similar problem occurs with older transformers if they are de-energized with switches prone to restrike (multiple restrikes drive the transformer flux to a very high level on de-energization, resulting in ultrasaturation on a subsequent energization [4]). Lowered harmonic blocking thresholds or increased harmonic

restraint as well as cross-phase blocking are sometimes applied to address this problem. However, these solutions may hurt dependability and speed on heavy internal faults with CT saturation and internal faults during inrush.

2.4 Internal faults during inrush

Moisture trapped inside the transformer slowly moves between the paper insulation and the oil, depending on temperature. A de-energized transformer may be cold, which leads to more moisture trapped in the paper insulation rather than dissolved in oil, degrading the insulation strength of the paper. In addition, the magnetizing inrush current during energization inflicts electromagnetic forces on the windings and may cause the coils to move. Dirt, animals, and debris may collect inside the transformer protection zone, outside the tank, while the transformer is de-energized. It is therefore possible that a transformer will fail during energization.

A faulty transformer being energized will still draw an inrush current and produce harmonics in the 87T differential signal. Therefore, the dependability of the 87T element may be compromised when using harmonics to address security during inrush, especially if the cross-phase blocking logic is applied or the harmonic blocking ratio thresholds are lowered.

2.5 Operating time for internal faults

Another issue that is less readily apparent is that the rise of the differential current at the inception of the fault will also generate false harmonics. These harmonics may slow down the differential element even if the CTs perform flawlessly. Fig. 1 illustrates the problem. Note that no harmonics are present in the current signal.

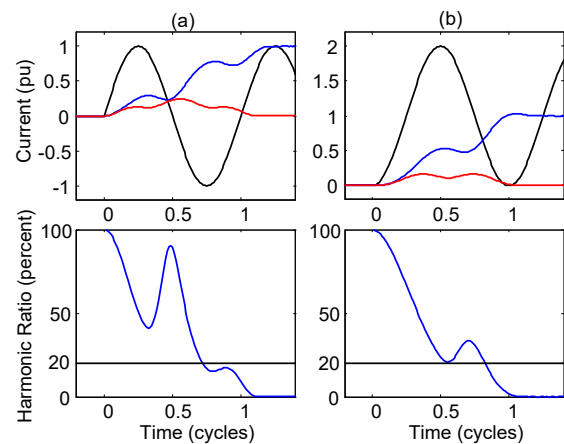


Fig. 1. Differential current free of any harmonics and the second-harmonic ratio measurement: symmetrical case (a), fully offset case with a decaying dc component (b).

Fig. 1 shows that the second-harmonic filter (red trace) is excited with the changing input signal and it takes approximately the length of the filter data window (typically one cycle) for the second harmonic to settle on a true value of zero. During the time the second-harmonic filter is excited, the second-harmonic ratio is large and the differential element will be blocked or restrained. These filter artifacts delay operation of the 87T element until the filter transient subsides.

This phenomenon is not limited to digital relays with digital filters. Any second-harmonic filter will show a similar behavior. A sudden change in the filter input (differential current) transiently contains a wide frequency spectrum and these transient frequency components excite the filter.

The phenomenon illustrated in Fig. 1 slows down operation for internal faults, but it is nonetheless desirable during inrush conditions. Fig. 2 shows the very first cycle of an inrush current, superimposed on fully offset and symmetrical fault currents of similar peak magnitudes. The inrush and the fully offset fault traces cannot be differentiated during the first three-fourths of a cycle. The signs of inrush are visible only toward the end of the first cycle. Therefore, a transformer differential relay must block or restrain during the first cycle unless a fault current appears with a magnitude so high that it allows a clear distinction between a fault and an inrush. On the other hand, the inrush and symmetrical fault current traces can be differentiated in as early as half a cycle. We will use this observation later for accelerated tripping.

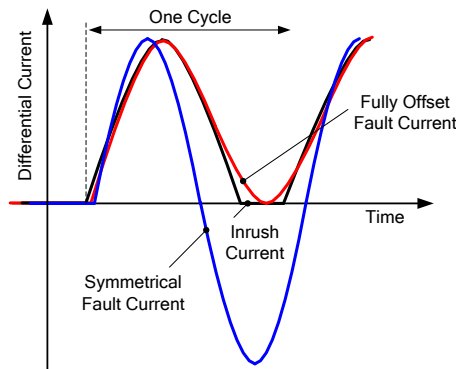


Fig. 2. Differential current during inrush and internal fault.

The spurious output from the harmonic filter due to the differential current rise provides the initial blocking required for security during inrush. During the time the harmonic filters are excited with the signal change rather than with the real harmonics (such as during the first cycle of an inrush current), the filter output may transiently decrease to a low value (see Fig. 1). Practical implementations often include logic to ride through such “holes” in the harmonic blocking signals.

3 Waveshape-based solution for transformer differential element security during inrush

One general technique based on the waveshape of the differential current uses the repeating periods of small and flat differential current (“dwell time”) present in an inrush current but not in a fault current. A modern digital implementation of this general principle is described in [3] and [4]. We summarize this method below.

Referring to Fig. 3, we observe that an inrush current exhibits periods of low and flat values. These periods last about one-sixth of a power cycle and repeat every cycle when the core briefly goes out of saturation. Moreover, for transformers with three-legged cores (i.e., without a low-reluctance magnetic path for a zero-sequence flux), these periods of low and flat current are aligned in time among all three phases.

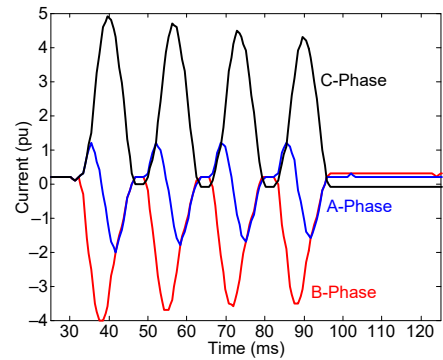


Fig. 3. Sample transformer currents during energization resulting in a false 87T operation.

We use the above observation for inrush detection and apply the logic shown in Fig. 4. Instantaneous values of the phase differential currents (87T IDIF A, B, and C) are the inputs to the logic, and the Boolean output, INRUSH, is the output (when asserted, the differential element shall not be allowed to operate). The algorithm uses information from all three phases but asserts a single output that applies to all three phases of the 87T element.

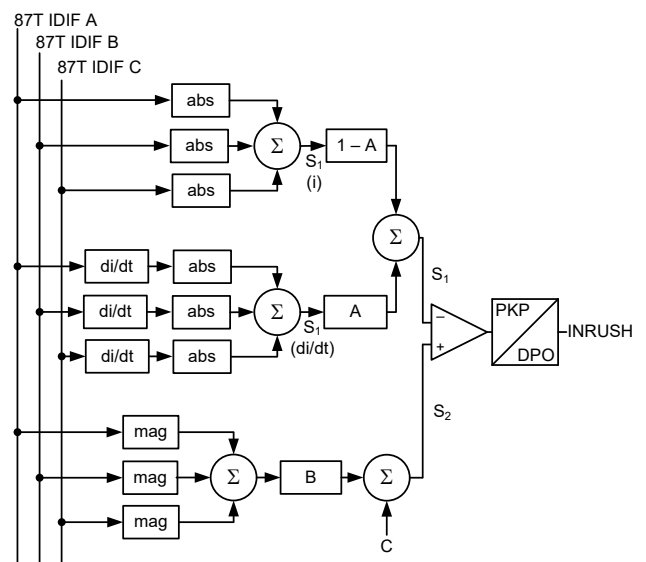


Fig. 4. Simplified block diagram of the waveshape-based inrush detection algorithm.

The algorithm runs on a sample-by-sample basis and works as follows:

- The absolute values of the instantaneous differential currents in all three phases are added to form the $S_1(i)$ signal. During inrush conditions, this signal is very low for the duration of the dwell-time periods because all three differential currents exhibit their dwell times at the same time. During internal fault conditions, this signal is high and reflects the fault current. If CT saturation occurs during inrush, the differential currents during dwell-time periods start departing from zero and $S_1(i)$ starts to increase slightly with time.
- The instantaneous differential signals are differentiated (di/dt). Because the inrush currents are flat during

dwelling-time periods, the result of the derivative is ideally zero. The absolute values of the derivatives are calculated next, and all three phases are summed to form the S_1 (di/dt) signal. Because all three inrush currents are flat during the dwelling-time periods, the S_1 (di/dt) signal is very low during inrush conditions for the duration of the dwelling-time periods. If CTs saturate during inrush, this signal may increase, as well as the S_1 (i) signal, but to a lesser degree.

- The logic adds the S_1 (i) and S_1 (di/dt) signals using the weighting factor A (between 0 and 1, consider $A = 0.5$ for example). The resulting S_1 signal is low during the dwelling-time periods of the inrush and high during internal faults. This signal is quite resilient to CT saturation during inrush. Increasing the value of A and biasing the operation toward using the derivative rather than the signal further increases the resilience of the algorithm to CT saturation during inrush.
- The logic measures and adds together the magnitudes of the phase differential currents to form an adaptive threshold for checking the value of S_1 . S_2 is a portion of the sum of the magnitudes (multiplier B) plus a constant, C (consider $B = 0.1$ and $C = 0.1$ pu).
- During inrush, once every power cycle for the duration of the dwell time, the S_1 signal is very low compared with the S_2 signal. The comparator checks the level of S_1 . If this signal is low for the duration of the pickup (PKP) time, then INRUSH is asserted and maintained for the dropout (DPO) time (typically one power system cycle). The DPO timer is required to wait for the next dwelling-time period in order to maintain reliable inrush detection.
- The logic applies the PKP time for the desired level of dependability for detecting inrush. For example, it can be set to one-sixth (or even as low as one-eighth) of a power cycle, allowing it to cope with cases of the second harmonic as low as 10 percent [3] [4].

Fig. 5 and Fig. 6 illustrate operation of the new algorithm by using an inrush case recorded in the field with a simulated fault current superimposed on the inrush waveform (in Fig. 5, the fault was added at about 72 ms after transformer energization). We expect the algorithm to block for the first 72 ms of inrush (security) and unblock shortly afterward (dependability).

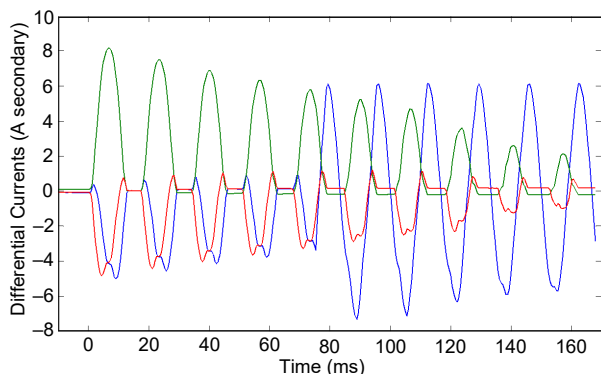


Fig. 5. Differential currents for an internal fault during inrush conditions.

Fig. 6 shows the key internal signals of the algorithm. As expected during inrush conditions, the S_1 (i), S_1 (di/dt), and S_1 signals are low for the duration of the dwelling-time periods. After the internal fault develops in the blue phase, the dwelling-time intervals have practically disappeared from the S_1 signal, though the other two phases continue to look like true inrush currents with clearly visible dwelling-time periods.

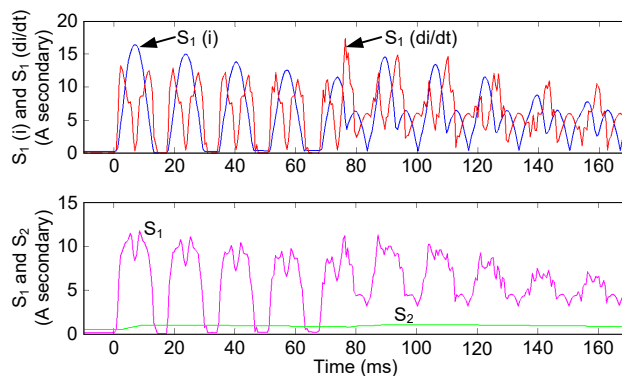


Fig. 6. S_1 (i) (blue), S_1 (di/dt) (red), S_1 (magenta), and S_2 (green) signals for the case shown in Fig. 5.

The S_1 signal drops repeatedly below the S_2 signal during inrush and stays consistently above the S_2 signal after the internal fault (Fig. 6). This means that during inrush conditions, the PKP timer picks up and maintains an INRUSH assertion. The last dwelling-time interval in the S_1 signal occurs at about 65 ms. If it was not for the internal fault, the next interval would occur at about $65 + 17 = 82$ ms. The DPO timer expires after about one cycle (around 82 ms), and because there is no new dwelling-time period present, INRUSH deasserts at 82 ms, allowing the 87T element to trip.

The method of Fig. 4 is not inherently faster than the harmonic-based method. The DPO timer in Fig. 4 maintains the INRUSH output for about a cycle after the last dwell time. Fig. 2 explains the reason for this in general. However, in the case shown in Fig. 5, the fault current is symmetrical, and we can accelerate tripping as explained in the following section.

4 Waveshape-based solution for faster and more dependable tripping

Our solution to improve the 87T operating time is based on a bipolar instantaneous differential overcurrent element. We first introduce this logic and follow with its applications for unblocking the 87T element and for unrestrained transformer differential protection.

4.1 Bipolar differential overcurrent element

The inrush current, if high, is unipolar. It becomes more symmetrical as the initial inrush current decays into a steady-state excitation current.

Fig. 7 shows the B-phase differential current from Fig. 5 superimposed onto two levels: a positive threshold and a negative threshold placed symmetrically with respect to current zero. During inrush conditions (first 72 ms), the differential current is negative and repeatedly crosses the

negative threshold (blue line in Fig. 7). However, it does not cross the symmetrically placed positive threshold (red line).

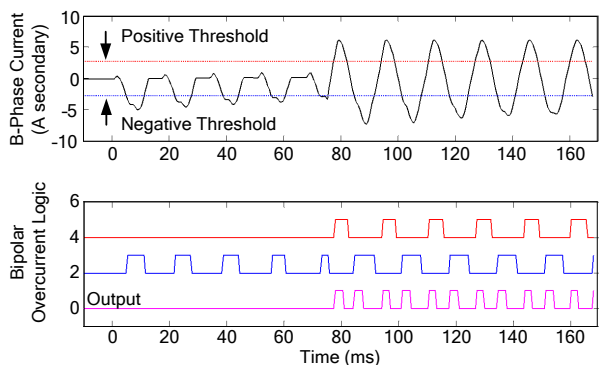


Fig. 7. B-phase differential current from Fig. 5 compared with positive (red) and negative (blue) thresholds.

When the internal fault develops (at 72 ms), the current crosses the negative threshold; shortly afterward, it crosses the positive threshold and so on. We use this observation to devise a new protection element as depicted in Fig. 8.

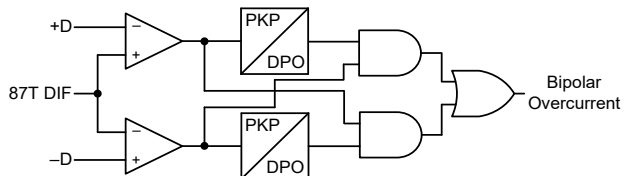


Fig. 8. Principle of operation of the bipolar differential overcurrent element.

The bipolar overcurrent element compares the instantaneous differential current (87T DIF) with the positive (+D) and negative (-D) thresholds. If the differential current is above the positive threshold for a short duration of time (PKP timer), a window, equal to the DPO timer, opens to wait for the current to decrease below the negative threshold. If it does, the current must be symmetrical, and therefore, it is not an inrush current. Mirror logic is used for the negative polarity. The PKP timer in Fig. 8 is introduced for security (one-eighth of a cycle, for example). The DPO timer is set to about one-third to one-half of a cycle.

The magenta trace in Fig. 7 is the output of the bipolar overcurrent element. The element asserts at about 78 ms (the fault occurred at about 72 ms).

Owing to the bipolar level check, this element does not have to be set very high to ensure security during inrush.

4.2 Inrush unblocking logic

We use a low-set bipolar overcurrent element to cancel the inrush blocking action in the 87T logic. If the differential current is symmetrical, it cannot be an inrush current, and therefore, it is safe to remove the inrush blocking action.

Before we allow the bipolar overcurrent element to cancel the inrush blocking action, we need to determine that the symmetrical nature of the current is not caused by CT saturation during inrush. CT saturation during inrush makes the differential current appear more symmetrical, but it does so

gradually, i.e., relatively slowly. In contrast, an internal short circuit results in a sudden change in the differential current. We check for a step change in the differential signal before we allow the bipolar overcurrent element to remove the inrush blocking action. Fig. 9 shows the inrush unblocking logic.

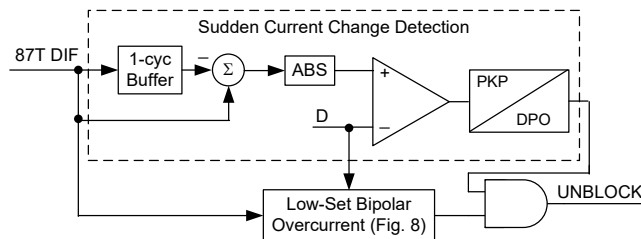


Fig. 9. Inrush unblocking logic using a low-set bipolar overcurrent element.

Fig. 10 explains how the inrush blocking action is removed in the 87T blocking logic and in the 87T restraining logic.

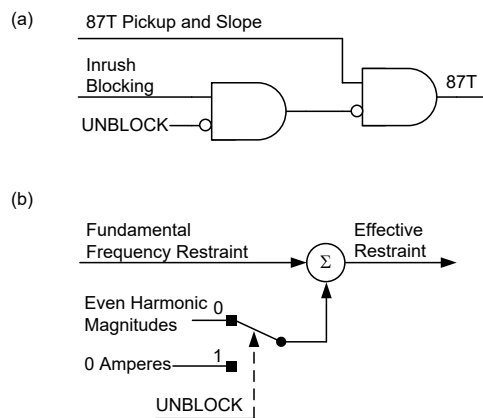


Fig. 10. Removing the inrush blocking action in the 87T blocking (a) and 87T restraining (b) elements.

We can expect the unblocking signal to assert as fast as one-half to three-fourths of a cycle – a half-cycle improvement in the operating time of the 87T element (see Fig. 11 for explanation).

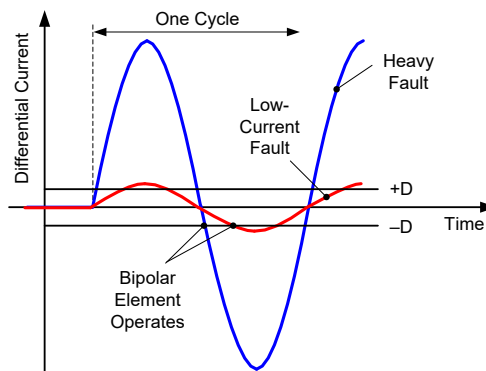


Fig. 11. Operating time for the bipolar overcurrent element for a symmetrical differential current.

4.3 Unrestrained differential logic

We also use the bipolar differential overcurrent element with a high-set threshold to trip unconditionally, i.e., as an instantaneous unrestrained (unbiased) element. This allows

fast 87T operation on heavy internal faults and takes advantage of the relatively low setting that is required for this high-set element. As shown in Fig. 11, we can expect this element to operate in half a cycle for heavy faults. For security, we can supervise this high-set directly tripping bipolar overcurrent element with the change in current, similarly to the unblocking application in Fig. 9.

4.4 Operating time benefits

Fig. 12 shows a comparison of the new algorithm with a reference relay for a range of internal fault conditions. We simulated in-zone faults with a varying level of the fault current and plotted the operating times as a function of the fault current in per unit of transformer nominal current. As expected for heavy faults, the inrush unblocking accelerates the 87T element by about half a cycle, and the bipolar unrestrained element trips in as fast as half a cycle. This trip time reduction can make a difference between the tank rupturing or staying intact.

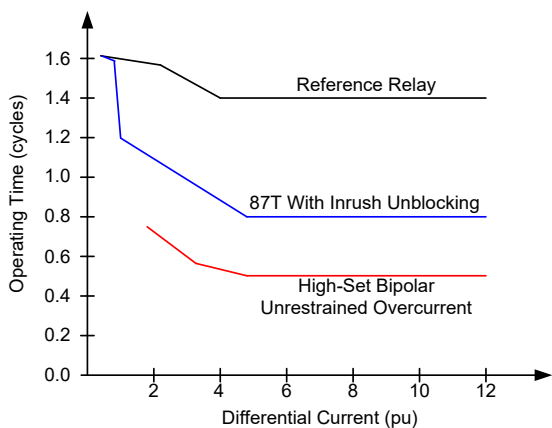


Fig. 12. 87T operating time as a function of the differential current.

4.5 Example of operation

Fig. 13 shows a field case of an internal fault in a 2250 MVA, 765/345/35 kV, multiwinding transformer. The installed relay operated in 1.1 cycles and the new algorithm would have operated in 0.5 cycle, a 0.6-cycle improvement.

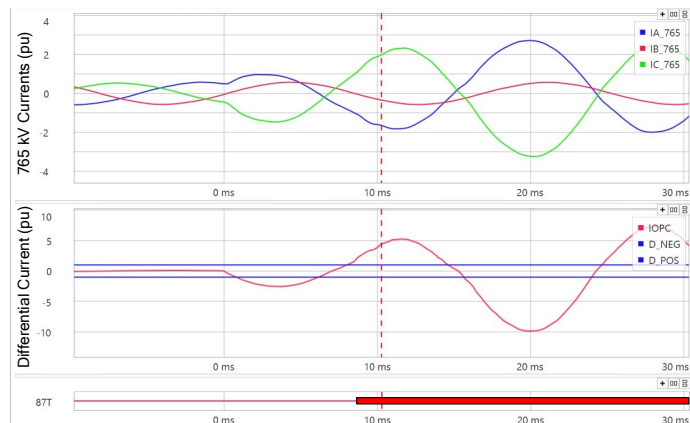


Fig. 13. Example of 87T operation for a 2250 MVA, 765/345/35 kV transformer.

5 Conclusions

Traditional harmonic-based solutions to 87T element security during inrush came from the limitations of the old relay technologies. These solutions served us well for older transformer designs with high levels of harmonics during inrush and operating time requirements for power systems with larger margins.

Numerical technology can examine the raw current sample data and directly identify the characteristics of inrush, making the past methods that rely on a surrogate measurement (harmonic content) obsolete.

Recently, transformer protection requirements have increased. New transformer core materials yield low levels of harmonics and call for better security during inrush, asset managers want to avoid tank ruptures (repairs, cost of oil spill cleanup), and decreased power system transient stability margins call for faster tripping times in general. Modern relay technology can deliver on these new requirements, providing adequate security during inrush as well as faster and more dependable operation for internal faults.

6 References

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