Traveling-Wave and Incremental Quantity Directional Elements Speed Up Directional Comparison Protection Schemes

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Presented at
RVP-AI 2018
Acapulco, Mexico
July 15–20, 2018

Originally presented at the
14th International Conference on Developments in Power System Protection, March 2018

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Keywords: traveling waves, incremental quantities, directional elements, permissive overreaching transfer trip.

Abstract

Directional comparison schemes provide dependable and secure power line protection. Directional elements are at the heart of directional comparison schemes. Voltage-polarized directional elements require voltages and currents to declare forward or reverse fault conditions. Recently, traveling wave-based (TW-based) directional elements have been introduced into line protective relays. Because of their construction, coupling capacitor voltage transformers (CCVTs) present challenges to these TW-based directional elements. This paper shows that TW-based directional elements can work with CCVTs by relying on the stray capacitances of the tuning reactor and step-down transformer. In this paper, we use field events captured during forward and reverse faults to analyze the performance of a permissive overreaching transfer trip scheme that combines incremental-quantity and TW-based directional elements for achieving end-to-end scheme operating times on the order of 4 to 6 ms.

1 Introduction

This paper (a shortened version of [1]) presents a new communications-based protection scheme that uses incremental-quantity and TW-based directional elements to make tripping decisions where CCVTs provide voltage signals to these elements. In this scheme, forward, overreaching, TW-based and incremental-quantity directional elements activate the transmission of a permissive trip signal to the remote end of the line. At the remote end, forward, overreaching, phase incremental quantity directional elements supervise the received permissive trip signal. The proposed scheme takes advantage of the fast TW-based elements, which operate within 150 µs, to speed up the trip decision and takes advantage of the incremental-quantity elements to provide security to the scheme. Additionally, the incremental-quantity elements provide phase selection for single-pole tripping (SPT) applications.

New protective relay technologies allow us to record signals from actual system faults at megahertz sampling rates. We use field events captured during forward and reverse faults at a 1 MHz rate to analyze the performance of the proposed permissive overreaching transfer trip (POTT) scheme.

Section 2 provides an overview of the principles associated with time-domain directional elements. Section 3 discusses the implementation of the fast and secure POTT scheme and the phase selection logic for SPT. Section 4 provides details about the field events captured on a 400 kV, 223.8 km (139.1 mi) series-compensated line for forward and reverse faults and analyzes the performance of the directional elements.

2 Time-domain directional element principles

Advancements in data acquisition and data processing allow for the development of ultra-high-speed (UHS) time-domain directional elements that are faster than phasor-based directional elements [1]. Next, we present the operating principles of these time-domain directional elements, which are part of a fast and secure communications-based protection scheme.

2.1 Incremental-quantity directional element

UHS time-domain line protective relays include incremental quantity-based directional elements that use instantaneous values of voltages and currents. This type of element is called TD32 in one implementation [2]; this element provides fast, secure, and dependable directional indication [3]. This directional element is part of a POTT scheme, and it supervises distance elements. It uses signals with frequency content on the order of hundreds of hertz.

TD32 is based on the product of the instantaneous incremental voltage and the instantaneous incremental replica current, which we call torque as it is referred to for electromechanical relays (see Fig. 1). We apply adaptive restraints for the operating torque using the concept of adaptive threshold impedances [4]. The TD32 element calculates the operating torque using a sign-inverted voltage so that the operating torque is positive for forward events. This element uses a positive restraining torque to check the forward direction and a negative restraining torque to check the reverse direction. The two restraining torques are equal to the product of the squared loop replica current and the corresponding threshold impedance magnitudes (TD32ZF for the forward threshold and TD32ZR for the reverse threshold).

The TD32 element integrates the operating and restraining torques. The integrators in this element are controlled by the starting logic as shown in Fig. 1. The restraining torques are integrated as soon as a disturbance is detected and as long as the incremental quantities are valid. To achieve security, the operating torque for any given protection measurement loop is integrated only if that loop was ready to operate prior to the disturbance and if the corresponding phase was involved in the fault.

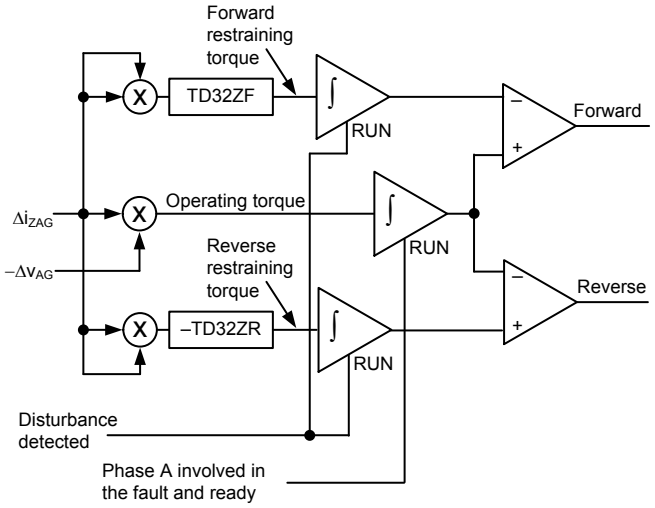

Fig. 1. Simplified logic of the TD32 element for the Phase-A-to-ground (AG) loop.

The TD32 element declares a forward event if the integrated (accumulated) operating torque is positive and greater than the integrated forward restraining torque. The TD32 element declares a reverse event if the integrated operating torque is negative and greater—in terms of an absolute value—than the integrated reverse restraining torque.

The outputs of the Fig. 1 logic diagram are supervised by sensitive incremental-quantity overcurrent elements and are conditioned according to the fault type for their application in the proposed POTT scheme.

2.2 TW-based directional element

TW-based directional elements that acquire voltage and current signals at megahertz rates have greater bandwidth requirements for CTs and CCVTs than phasor-based directional elements. Wide bandwidth allows for considerable improvements in the operating speeds of these elements [4]. Dommel et al. [5] and Johns [6] proposed TW-based directional elements that require high-fidelity voltage measurements that are not available in typical substations. However, in most cases, CCVTs can measure the first voltage TW (because of the interwinding capacitance across the step-down transformer and the interturn capacitances across the tuning reactor of the CCVT). This allows for a new type of TW-based directional element (called TW32) that takes advantage of the information in the first voltage and current TWs; this new element acquires voltage signals from conventional CCVTs. The following are the implementation details of this element [3] [7]. In this implementation, we use a differentiator smoother filter to extract TWs from the raw voltages and currents [8].

The TW32 element uses phase voltage and current TWs and calculates the product of the current TW and the sign-inverted voltage TW (so that the product is positive for forward events) for each phase, as shown in Fig. 2. Then, the element integrates this product over time to obtain the energy associated with the first TW. For security, the logic of the TW32 element enables the integrator only if the voltage and current TWs are above their corresponding minimum levels. The logic checks the output of the integrator after the TW32WD timer expires. The integration lasts only for a few tens of microseconds because the TW32 element is designed to respond only to the first TWs.

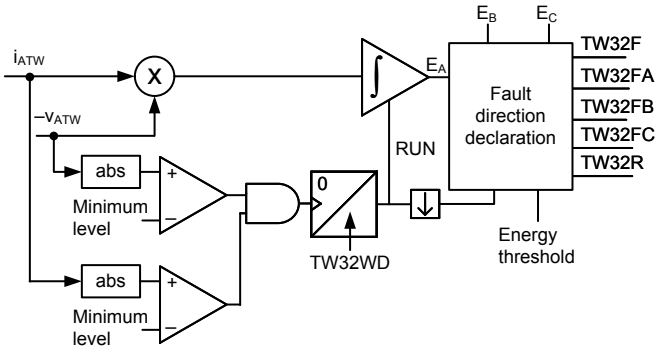

Fig. 2. Simplified logic of the TW32 element.

TWs associated with a line fault can arrive at the relay location from the fault and from the network elements behind the relay. Each TW coming from the line direction integrates up, and each TW coming from behind the relay integrates down. The first TW is higher in magnitude than the subsequent reflections. As a result, we have confidence that the integrated value is a reliable indication of the fault direction even as multiple reflected TWs are integrated over the time period TW32WD, such as is the case when the fault or the discontinuities behind the relay are located very close to the relay.

When the TW32WD timer expires, the integration is complete (see Fig. 2). At the falling edge of the timer, the fault direction declaration logic uses the accumulated values of the per-phase TW energies (E_A, E_B, and E_C) for determining if the event is in the forward or reverse direction. The energy must exceed the security threshold, ENRGYTH, for the logic to assert the forward or reverse bit. The TW32 logic determines which are the maximum and minimum energy values (ENRGYMX and ENRGYMN, respectively) from among the three per-phase energy values (E_A, E_B, and E_C). The element declares a forward event or fault by asserting the TW32F bit if the following conditions are met:

- |ENRGYMX| > |ENRGYMN|
- ENRGYMX > ENRGYTH

The element declares a reverse event or fault by asserting the TW32R bit if the following conditions are met:

- |ENRGYMN| >= |ENRGYMX|
- ENRGYMN < –ENRGYTH

The logic asserts the phase-segregated forward elements (TW32FA, TW32FB, or TW32FC) based on which phase energy value corresponds to the ENRGYMX value. This way, the logic provides sufficient fault phase identification for single-phase-to-ground faults. This logic identifies one of the faulted phases for multiphase faults. The operating time of this element is on the order of 150 µs or less. The TW32 element may not assert for faults near the voltage zero-crossing, for high-resistance faults where the change in voltage is small, or with some CCVTs that have limited bandwidth. The TD32 element ensures dependability under these operating conditions.

3 Fast and secure POTT scheme

In our implementation, the TW32 elements are fast and very sensitive for detecting events [2]. They can detect reactor and capacitor switching, nearby lightning, and other events that might compromise the security of the tripping scheme. The TD32 elements are not as fast as the TW32 elements, but they are very secure and dependable. How can we take advantage of the speed of the TW32 elements without sacrificing scheme security?

In this section, we describe a POTT scheme suitable for single- and three-pole tripping applications that uses the TW-based directional elements for speed, the incremental-quantity directional elements for reliability, and the incremental overcurrent elements for security.

The POTT scheme includes the following logic:

- *Key Transmitter Logic.* This logic sends a phase-segregated permissive signal to the remote line terminal when a forward event occurs.
- *Receiver Logic*. This logic compares the received permissive signal with the local directional element to provide trip permission.
- *Phase Selection and Tripping Logic*. This logic selects the phases to trip and trips the selected phases if there is a trip permission signal.

3.1 Key transmitter logic

The key transmitter logic activates phase-segregated transmission bits (KEYA, KEYB, and KEYC) to send a permissive signal indicating the presence of a forward event to the remote relay (see Fig. 3). The logic uses the phase-segregated forward directional elements TD32F and TW32F to assert the transmission bits. The TW32F element makes the directional declaration faster than the TD32F element, which typically results in speeding up the permissive signals by 1 to 3 ms.

Additionally, the POTT key logic asserts the TDRBA bit when the TD32 element detects the occurrence of a reverse event on Phase A in order to block the permissive signal transmission. If the reverse event indication lasts longer than a very short period of time (e.g., 2 ms), the TDRBA bit remains asserted after the TD32 reverse event indication de-asserts for an extra period of time (e.g., 80 ms). This extra delay is enough for the remote overreaching elements and communications channel to reset after the prior reverse fault clears, in case the reverse event is a fault.

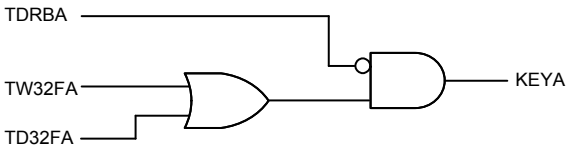

Fig. 3. Key transmitter logic for accelerating the POTT scheme.

3.2 Receiver logic

The local relay receives the phase-segregated permissive bits (PTA, PTB, and PTC) through the communications channel. These signals are supervised by the TD32 forward indication but not by the TW32 forward indication. The permissive signals arrive after a channel delay, and at that time the TD32 elements are already asserted and the scheme does not need the TW32 acceleration. By not using the TW32 elements on the receiving end, the scheme is more secure. Phase-segregated directional overcurrent elements, through the use of the OCTPA, OCTPB, and OCTPC bits, supervise the POTT scheme permissive trip signal for security during switching operations, as Fig. 4 illustrates. The current reversal bits (TDRBA, TDRBB, and TDRBC) supervise the POTT scheme permissive trip signal for security during the clearing of a fault on a parallel line. The Phase A-supervised permissive bit PTRXA asserts if there is an overcurrent condition on Phase A and if the corresponding current reversal bit is not asserted.

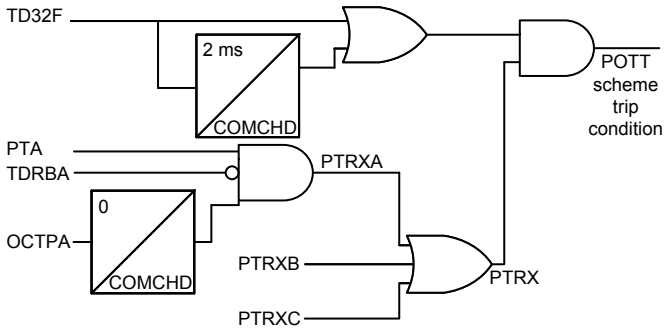

Fig. 4. Receiver logic provides security to the POTT scheme.

The receiver logic extends the assertion of the TD32F bit (the OR combination of TD32FA, TD32FB, and TD32FC) according to the communications channel delay timer COMCHD (e.g., 15 ms) to indicate the presence of a forward event. This extension ensures that the local forward event indication based on incremental quantities is present when the remote trip permissive signal is received after the channel delay. The logic also extends the OCTPA, OCTPB, and OCTPC bits for the same reason. A POTT scheme trip condition is granted when at least one of the PTRX bits asserts and the local forward event indication TD32F is asserted.

3.3 Phase selection and tripping logic

Fig. 5 shows the phase selection and tripping logic that executes the trip in Phase A, B, or C for single-phase faults or in all three phases for multiphase faults. The logic selects Phase A for tripping if the POTT scheme operates in Phase A, as signaled by the assertion of the permissive trip signal in Phase A (PTRXA) coinciding with the pickup of the TD32 forward element in Phase A (TD32FA). For multiphase faults, the TD32 element asserts the TD32F bits of all the phases. The logic executes trips in all phases if all the previously mentioned conditions are met. The trip seal-in and unlatch logic asserts the trip outputs TPA, TPB, and TPC while current is flowing through the corresponding pole of the breaker; a predefined time determines the minimum assertion time of the trip outputs (e.g., 200 ms).

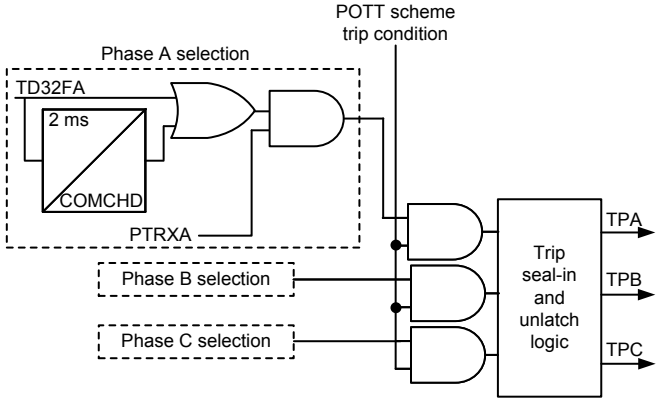

Fig. 5. Phase selection and trip logic for the POTT scheme.

In summary, the TW32 element speeds up keying of the permissive trip signal at the transmitting end if there is no current reversal condition. Note from the parallel line discussion that for external faults, both line ends assert the TW32 elements in the reverse direction and no key from the TW32 element is expected at all. At the receiving end, phase overcurrent elements supervise the permissive signal; a POTT scheme trip condition is granted if the TD32F bit is asserted and there is no current reversal condition. Per-phase tripping occurs when a POTT scheme trip condition exists and the corresponding phase has been selected for tripping. The logic selects a phase for tripping if the per-phase TD32F element and the corresponding PTRX bit coincide. Overall, the receiving end logic provides the necessary scheme security without slowing down the scheme operating time. The POTT scheme takes advantage of the communications channel delay. The very fast overcurrent and incremental-quantity directional elements have enough time to detect the fault condition by the time the permissive signal arrives at the terminal even when using a very fast teleprotection channel.

4 Field experience

Comisión Federal de Electricidad (CFE), the electrical utility company of México, installed two relays that include the directional elements described in Section 2, as well as an incremental quantity-based underreaching distance element, a TW-based differential element, and fault location functions. This field installation has the following purposes:

- Evaluate new time-domain protection principles that offer faster tripping times than traditional principles. High-speed tripping minimizes equipment damage, increases stability margins, and increases personnel and public safety.
- Evaluate the settings simplicity of relays that use time-domain principles [7].
- Analyze CCVT response to high-frequency signals.
- Evaluate the accuracy of the TW single-end fault locating method [9].
- Analyze high-resolution oscillography records and evaluate the possibility of using the recorded information for predictive maintenance of lines and other primary equipment.

CFE decided to verify the security of the new time-domain protection elements in a 400 kV, 223.8 km (139.1 mi) series-compensated line that connects substations Minatitlán Dos (MID) and Temascal Dos (TMD); this transmission line is in a region with a high incidence of lightning events. During the first eight months of evaluation, the new time-domain relays have experienced four internal faults, two external faults, and several equipment switching events. The protection elements have been secure and dependable during the evaluation period. The details for each fault are as follows:

- *January 7, 2017 internal AG fault*. The TW32FA and TD32FA bits asserted in 138 µs and 1.2 ms, respectively, and keyed the communications channel at MID. The event at TMD was overwritten with transient events.
- *January 15, 2017 external AG fault*. For the fault behind TMD, the TD32RA bit asserted in 1.7 ms at TMD, and the TD32FA bit asserted in 1.9 ms at MID. The TW32 elements did not operate for this fault.
- *January 16, 2017 external CG fault*. For the fault behind MID on the 115 kV network, the TD32RC bit asserted in 1.8 ms at MID, and the TW32FC bit did not assert at MID. The event at TMD was overwritten with transient events.
- *March 28, 2017 internal CG fault*. The TW32FC and TD32FC bits asserted in 106 µs and 1.39 ms, respectively, and keyed the communications channel at TMD. The event at MID was overwritten with transient events.
- *May 4, 2017 internal CG fault*. The TW32FC and TD32FC bits asserted in 105 µs and 1.1 ms, respectively, and keyed the communications channel at MID. The TD32FC bit asserted in 1.055 ms and keyed the communications channel at TMD.
- *August 23, 2017 internal AG fault*. The TD32FA bit asserted in 8.75 ms and keyed the communications channel at MID. The TD32FA bit asserted in 7.8 ms and keyed the communications channel at TMD. The TW32 elements did not operate for this fault because of the high fault resistance. The TD32 elements operated 9 ms faster than the conventional directional elements.

Fig. 6 and Fig. 7 show the currents and voltages captured at MID and TMD and the time-domain protection element operation for the May 4 internal CG fault. We can observe the assertion of the TW32FC, TD32FC, and KEYC bits at MID and of the TW32FA, TD32FC, KEYA, and KEYC bits at TMD. Notice that the TW32FA bit asserts at TMD but the TD32FA bit does not assert at MID; therefore, the assertion of the TW32FA bit does not compromise the scheme security.

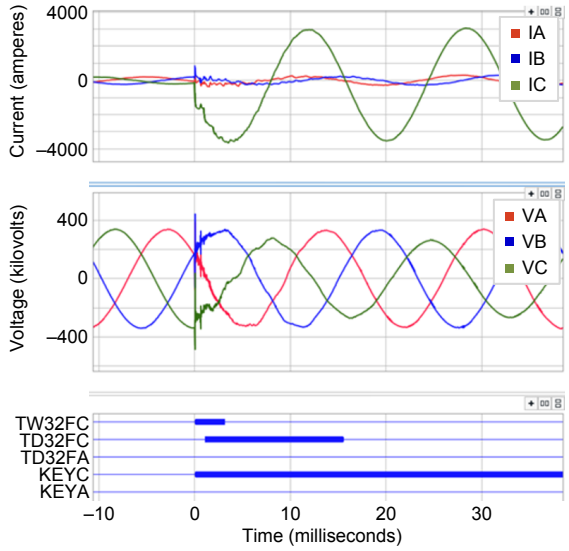

Fig. 6. Currents and voltages captured at MID and the time-domain protection element operation for the internal fault on May 4.

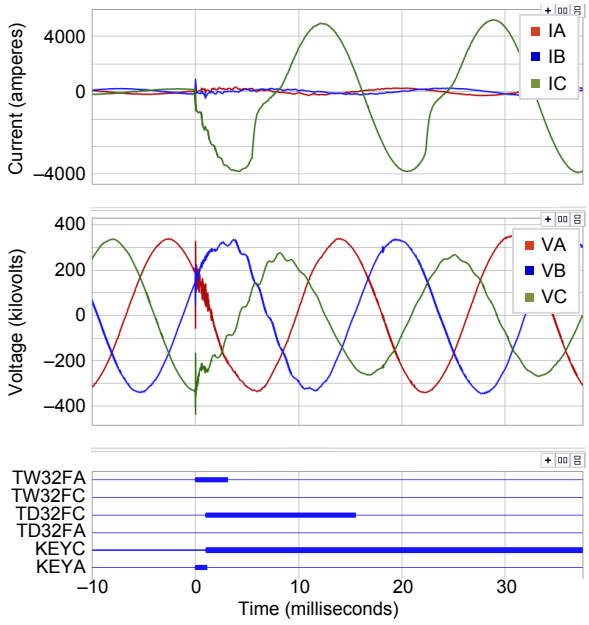

Fig. 7. Currents and voltages captured at TMD and the time-domain protection element operation for the internal fault on May 4.

Fig. 8 shows the TW current and voltage signals captured at MID.

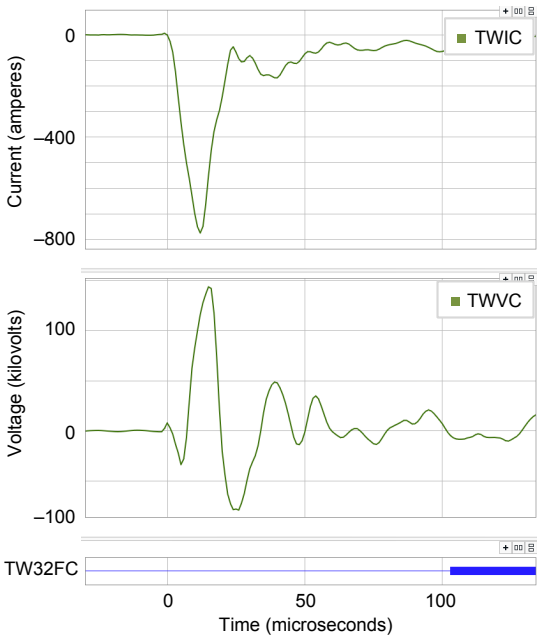

Fig. 8. TW current and voltage captured at MID and the TW32 protection element operation for the internal fault on May 4.

Fig. 9 shows the incremental quantity voltage and current signals captured at MID. The plot also shows the assertion of the TD32FC bits at both terminals.

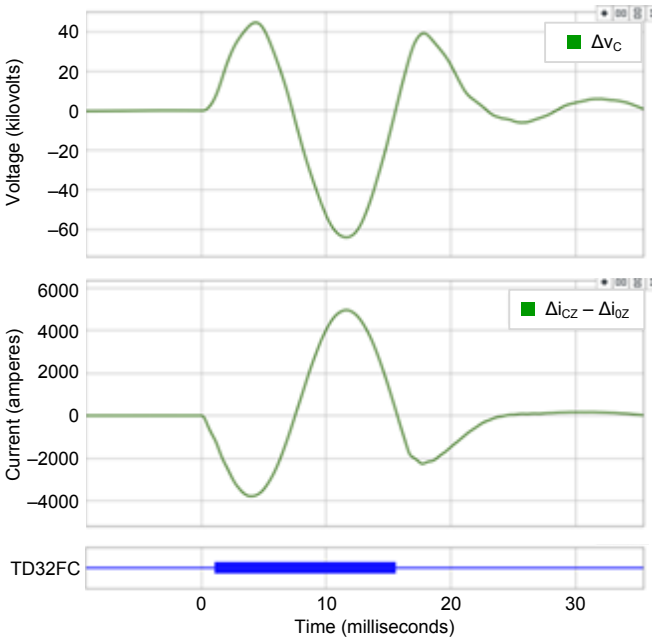

Fig. 9. Incremental voltage and replica current of the CG loop captured at MID and the TD32 protection element operation for the internal fault on May 4.

5 Conclusion

During the evaluation period, the CFE network where the time-domain protective relays are installed experienced four internal and two external faults. The TW32 elements asserted forward in three of the four internal faults and did not assert forward at all for the external faults. The fastest operating time was 105 µs and the slowest was 138 µs, with the average operating time being 116 µs. The TW32 element operations show that for some of the internal faults, the CCVT secondary voltages provide enough signal information for proper element operation, which speeds up the POTT scheme. However, different fault conditions, including factors such as point on the wave, fault resistance, distance to external faults, and CCVT response, can lead to weak and distorted voltage TWs that compromise the dependability of this element. As described in the paper, the POTT scheme includes TW32 elements for speed, but it relies on the slightly slower (by 1 to 3 ms) TD32 elements for dependability and security. The TW32 elements were secure for all external faults and transient events.

The TD32 elements operated correctly for all faults, and they did not operate for any voltage or current transient conditions during switching and lightning events. The fastest operating time was 1.055 ms and the slowest was 8.750 ms (for the high-resistance fault on August 23 with very slow current increase), with the average operating time being 2.966 ms for all faults.

The field cases presented in this paper show that the POTT scheme that uses TW32 elements to speed up the transmission of the permissive signal and TD32 elements for phase selection and trip supervision reduces scheme operating times while maintaining security and dependability.

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